09 - Energy Management (*Gestion de l'Energie* — GE)

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Research Teams: Power Management System Integration (ISGE), Energy and Embedded Systems (ESE)

Keywords: power devices, energy conversion, energy management, power integration, energy harvesting, robustness, predictive reliability…

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1 Presentation

1.1 Objectives and Scientific Positioning

One of the big challenges that our society will have to face over the next decade is related to energy issues. Worldwide, most of the energy is consumed into transports and buildings, both residential and industrial, thus resulting in a significant increase of CO_2 emissions and global warming. The majority of this energy is generated by non-renewable and non-environmentally friendly coal, fossil fuel and natural gas. In the objective of a sustainable development, the widespread of alternative energy sources in transportation and buildings is the solution that will require a major paradigm shift in the power industry:

- Transports will have to become more electrically driven thus demanding for new generations of power devices and converters.
- For a large penetration of renewable energies, it is more appropriate to move from a centralized generation approach to a distributed one.

The information economy of the 20th century was built around silicon technologies to revolutionize computing and communication. In the same way, silicon and semiconductors in general will play a key role in the emerging energy economy of the 21st century for the transmission, distribution and consumption of electricity. Concurrently, the advances in micro and nanotechnologies allow a drastic miniaturization of systems for power generation and management, thus increasing the autonomy of embedded systems and making possible the dissemination of wireless sensor networks in a large variety of applications so called "ambient intelligence". This last objective requires, on the one hand, the development of innovative approaches for energy harvesting coupled to low-power converters and on the other hand, the integration of high-density storage devices.

The research activities of the Energy Management Theme deal with the optimization of energy efficiency, robustness and reliability of conversion architectures dedicated to electrical grid - including alternative energies - to transport vehicles and to embedded systems, from elementary power devices to full modules. Main research areas are threefold:

- Power integration: from device to system
- Robustness and reliability: ESD/EMI, radiation hardening, electrothermal modeling
- Energy autonomy of embedded systems

These research activities are carried out with the support of LAAS-CNRS technology platform that is part of the RENATECH network and is the only one with the label "Energy system integration". In addition, we have dedicated electrical characterization platforms (ESD, EMC, power) and an experimental building, ADREAM, with 100kWp photovoltaic platform.

On the University of Toulouse campus, LAAS-CNRS has complementary activities with LAPLACE laboratory and is member of 3DPHI GIS (http://www.3dphi.fr/), which has setup a technology platform dedicated to hybrid power integration, in perfect complementarity with LAAS-CNRS technology platform. At national level, we are part of SEEDS GDR and have several cooperative projects in the field of power electronics systems with G2elab, AMPERE, LAPLACE, LPCIM, CEA LITEN and INES to develop new integrated devices, functions and converters with several complementary research activities on very high voltage devices, on the one hand, and very low voltage/high current solutions, on the other hand.

Internationally, we are in competition with CNM-Barcelona whose specificity is SiC, the University of Cambridge (UK), the Fraunhofer Institutes (IISB and IMS, ISE in photovoltaic field) in Germany, EPFL of Lausanne, Tyndall in Cork in passive components and energy harvesting, Tokyo Tech, the Hong Kong University of Science, University of Toronto, CPES from Virginia Tech (USA), University of Colorado and from Rensselaer Polytechnic Institute (USA) in converters and associated controls. The leadership of our teams is well recognized worldwide: partnership in WIDELAB LIA (AMPERE, CNM, LAAS) on wide bandgap semiconductors, participation to several FP7 European projects (one as coordinator), involvement in Next-PV LIA with Tokyo Tech, invited talks, active involvement in program committees of major conferences of the field and in international associations (ESD Association, Electrochemical Society…).

1.2 Organization and Life

The Energy Management (GE) Theme is organized in two complementary research teams:

- Energy Management System Integration (ISGE)
- Energy and Embedded Systems (ESE)

ISGE team mainly works on the challenges of power integration, both monolithic and hybrid, from design and technological realization of active and passive power devices to innovative architectures of conversion systems.

ESE team tackles the challenges of the management of energy in the environment either to capture it to improve energy autonomy or to increase the immunity of the embedded electronics system to disturbances (electrothermal management, electrostatic discharges (ESD), electromagnetic interferences (EMI)).

1.2.1 Activity Profile

Table 1 hereafter depicts the activity profile for the Theme. Since energy is a strongly multidisciplinary societal challenge, to carry out its research activities, GE Theme has strong and well-balanced interactions with both academic and industrial partners.

Table 1: Activity Profile

%	Academic research	Interaction with environment	Research Support	Training
GE	45	25	10	20

1.3 Salient Facts

Over this period, there were major evolutions both in terms of recruitment and of research topics. Our major activity on innovative power devices, originally focusing on silicon, evolved towards wide bandgap semiconductors (GaN, SiC, diamond). Within the framework of ADREAM transverse project, we participated to the definition of the energy aspects of an experimental building, which opens a new field of research related to the efficient management of renewable energies in a microgrid dedicated to urban applications.

In addition, two new research topics started during this period:

- EMC immunity and related long-term reliability.
- Energy autonomy of wireless systems: energy harvesting and microstorage.

Hereafter are summarized some salient facts organized by research topic.

Power integration:

- State-of-the-art results for innovative wide bandgap power devices:
    - GaN HEMT on 6” silicon wafer: 1000V breakdown voltage and 2.5 mΩ.cm^2 specific on-resistance.
    - Diamond Schottky diodes: 3.8 kA/cm^2@5V and 3.75 MV/cm maximum breakdown electric field.
- CNRS Bronze medal in 2011 awarded to Magali Brunet for her remarkable results in the field of passive devices and pioneering work on microsupercapacitors.
- Strong innovative activities on renewable energy converters and their management with several academic collaborations, CEA and Total S.A contracts (ANR LiPV, PHD CiFRE) and the creation of the 100 kWp PV platform of ADREAM building.
    - Doc’Innov 2011 Price for the best innovation research work: J-F Reynaud Ph.D. thesis.
    - Innovative work in the field of lifetime improvement of photovoltaic power converters: best paper award at conference IECON 2012, Montréal, 10/2012.
    - GEET best thesis award for original work related to PV converter efficiency under shading conditions: Y. El Basri, 2013.
    - 4 international patents with Total S. A.
    - Involvement into two Research Federations: SH&HD (co-direction: C. Alonso) and FEDESOL related to renewable energies.
- GEET best thesis award and UPS Physics Award of « Académie des sciences, inscriptions et belles lettres » of Toulouse for the work related to the design of a monolithic self-switching power device: F. Capy, 2010.
- Member of LABEX GaNex, national network on GaN.
- WISEA Alliance: IISB Fraunhofer Institute, Nuremberg University and CEMES (as a result of fruitful MOBISiC project)

Robustness & reliability:

- Strong activity in the field of ESD with 7 PhD theses defended, the development of original test benches (near-field scan, Transient TLP, double pulse TLP) and the proposal of a behavioral methodology for system level ESD modeling that is currently being discussed at ESDA standard committee for becoming a new standard.

- Pioneering work on characterization and modeling of the impact of ageing on EMC properties (both emission and immunity): ANR JC EMRIC, 14 publications in journals, best paper award at EMC Compo 2013.
- Original radiation hardening techniques for IGBT devices.
- Adaptive and distributed electrothermal and thermo-mechanical modeling methodologies for predictive reliability simulation of advanced power devices in harsh environment: 4 ANR projects (FIDEA, MHYGALE, MOSiSTAR, REMAPODE). Transfer of this methodology to smart power design center of Freescale (Toulouse).
- GEET best thesis award for pioneering work on ESD protection devices operating at high temperature: H. Arbess, 2012.

Energy autonomy:

- Two new research topics, energy harvesting and microstorage, with a strong activity: 2 FP7 projects, one as coordinator, CORALIE “Investissements d’avenir” project, ANR JC MIDISTOCK, 1 FUI and 1 FNRAE.
- State-of-the-art results for microsupercapacitors integrated on silicon: up to 675 mF/cm^2 specific capacitance and extremely high power densities (700 mW/cm^2).
- Valorization and transfer of results obtained within SACER project: implementation of photovoltaic powered wireless battery-free sensors for flight tests. Successful flight tests realized in June 2014 on an Airbus A321.
- Two original techniques for energy harvesting in the harsh environment of aeronautics:
  - Use of a phase change material (water) in the case of thermal gradients (FNRAE AUTOSENS): 15J harvested over one-hour flight.
  - Proof of concept of efficient aeroacoustic energy harvesting.

2 Scientific Production

Given the large range of energies associated to each application (from mobile electronics to electrical traction) and the corresponding current and voltage levels, the challenges of power integration and management are different from those of signal processing systems. As a result, the design of new power devices and their integration requires a top-down approach starting from the application needs.

Our strategy then consists in a global analysis of the different aspects of the final system: converter architectures, active and passive devices, energy autonomy and environment constraints, protection and robustness to propose innovative concepts and related technology solutions. This approach is supported by a strong expertise in modeling, design, realization and characterization in the field of energy systems.

As silicon is a key semiconductor material for embedded electronic systems, we are still carrying out research on silicon-based power devices with the objective of pushing away the limits of silicon. To this aim, we have chosen to develop specific 3D silicon technologies (deep trenches, double-side lithography...) to take advantage of the full semiconductor volume and to design bidirectional switches. Introducing new materials (magnetic, high-K dielectrics…) in the silicon process is also a key step. Moreover, to fulfill the requirement of a higher switching frequency for power conversion, we study new topologies based on interleaved structures and their digital control laws.

Nevertheless, further increasing power device performance requires a technological breakthrough. We have then chosen to study wide-bandgap devices (gallium nitride, diamond, silicon carbide) that offer the possibility to overcome both temperature and power management limitations of silicon.

Regarding power systems, to validate in real conditions new concepts on the management of renewable energy and its storage, we have designed a “zero-energy” building, named Georges Giralt, which is an innovative experimental platform with 7000 sensors. Within the framework of ADREAM transverse axis, this platform was designed to carry out real-scale experimental validation of multidisciplinary research projects related to energy issues.

Finally, with the development of energy storage micro-devices (micro-supercapacitors), we are aiming to provide energy storage on chip, which can be co-integrated with its control circuit and/or the sensor requiring power. This microstorage activity was concurrently started with the one in the field of energy harvesting that focuses on providing efficient energy management for battery-free wireless sensors. These two activities are tightly related, the main objective being to provide new breakthroughs for energy-autonomous wireless sensors both in terms of technological integration and energy-efficient architecture of the node.

The activity of robustness and reliability is mainly related to power devices and systems but also extends to any other type of electronic system. The approach is first to get a thorough understanding of the involved physical mechanisms via multi-physics modelling and simulation as well as dedicated characterization. From this knowledge, efficient protection strategies such as radiation hardening techniques or novel ESD/EMC protections can be devised to improve the system immunity to the related disturbances. Another important challenge is to provide predictive simulation methodologies.

Electromagnetic compatibility (EMC) is a new activity in the theme started in 2011 with the arrival of two researchers whose integration was easy given the strong convergence between ESD and EMC methodologies. The common approach consists in developing dedicated characterization techniques with reduced intrusiveness and predictive modelling methods. Two complementary approaches are contemplated: on-chip sensors for their good resolution and large frequency range as well as near-field scan for system level analysis. The proposed modeling ESD/EMC methodology aims at being as generic as possible by providing a hierarchical and behavioral approach from chip to printed circuit board (PCB) or even electronic equipment.

Regarding electrothermal and thermo-mechanical strain management, the main challenges are related, on the one hand, to multi-physics phenomena and on the other hand, to multi-scale issues either temporal or spatial. To cope with these problems, our methodology is based on 3D electro-thermal simulation, to investigate the involved failure mechanisms. To this aim, a new procedure to create communication between electrical modelling solver and thermal one has been developed.

2.1 Power Integration: *From Device To Systems*

2.1.1 Passive Devices

Nowadays, the trend toward miniaturization of mobile electronic products requires higher power density for systems such as DC/DC converters. Up to now, power semiconductors and control circuits can be fully integrated but the passive components, especially inductors, are still an obstacle for further reducing the size of these converters. For future power system on chip with high efficiency and high power densities, passive components should be integrated onto silicon and show high specific values, together with high DC current, reasonable breakdown voltage (depending on the system output power) and most importantly low losses at relatively high operating frequencies (> 1 MHz). Research activities in this field are focused on high-density integrated capacitors and micro-inductors.

In terms of capacitor topology, 3D structuration combined with the deposition of high-k dielectrics is necessary to reach very high specific capacitance values (above 500 nF/mm²) [*RVSI12694*]. The deposition of conformal high-k dielectrics in 3D high-density structures made of submicron micropores is a real challenge. First structures with $SrTiO_3$ high-k dielectrics were realized in the context of a collaborative industrial project (PRIIM) and electrically characterised at LAAS-CNRS. For $SrTiO_3$ deposited by MOCVD (at LEMHE Orsay) from a single source hetero-metallic precursor, good dielectric properties were obtained but deposition is not conformal. For $SrTiO_3$ deposited by Atomic Layer Deposition (ALD) (at TU Eindhoven), from two precursors, step coverage is improved. These studies of $SrTiO_3$ high-k material allowed identifying that crystallization and dielectric properties largely depend on the Sr/Ti ratio, the sub layer employed (Ti, Pt, Ru) and the annealing conditions (temperature and gas: O_2 or N_2). This work will continue on recently acquired ALD equipment at LAAS-CNRS.

Concerning micro-inductors, the activity focused on the fabrication of ferrite-based inductors on silicon for hybrid integration in low power (few Watts) DC/DC conversion. This work was carried out in cooperation with LAPLACE, with the support of 3DPHI platform and within the framework of PRIIM OSEO-funded project coordinated by IPDIA Company. Due to their high resistivity, soft NiZn ferrites are good candidates for magnetic cores working in the 5 to 10 MHz switching frequency range. The inductors were fabricated using micromachining and assembling techniques, and the process consisted in a sintered ferrite core placed in between thick electroplated copper windings. The cores produced by three methods (commercial tape-casted films, home-made ferrite powder or without magnetic layers) were characterized with respect to their magnetic properties, microstructure, composition and losses by Vibrating Sample Magnetometry, Scanning Electron Microscopy and impedance analysis. At 6 MHz, 890 nH of inductance has been recorded with a 1.2x2.6x0.2 mm^3 core using a commercial film (ESL 40011 - Electro-Science® Company) corresponding to ~290 nH/mm^2 [*MAI13442*]. Moreover, we developed a new simulation tool dedicated to the design of conductors for multi-layers and high frequencies, including several parasitic effects and interactions. Several researchers of our lab and the TEAM service now use this tool.

The co-integration of an LC filter was also demonstrated and successfully implemented in a real converter [*RVSI10568*].

2.1.2 Active Devices

Although we still carry out research activities on silicon power devices (Superjunction MOSFETs and thyristors), the main research activities are now focused on wide band gap (gallium nitride, silicon carbide, diamond) devices.

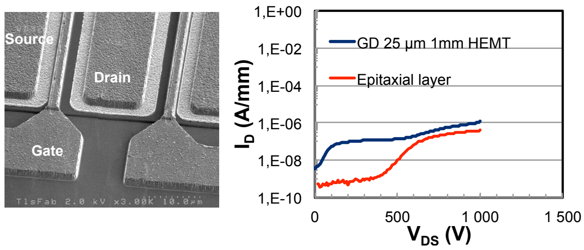

Figure 1: Photograph of realized HEMT GaN device and breakdown voltage measurement (BV ~2µA/mm@1kV).

Concerning diamond, a platform of simulation was developed to design high-voltage and high-temperature diamond device [*RVSI10100*]. From results of simulations, Schottky diodes were realized by deposition of nickel (Ni) on p- homoepitaxial layer of diamond [*RVSI11643*] [*TH11899*]. Their electrical characterization under operation temperatures ranging from 300K to 625K resulted in a forward current density close to 3.2 kA/cm^2 @ 5 V and a maximum breakdown electric field of 3.75 MV/cm. These results, among the best in the state-of-the-art [1], also showed thermal stability of diamond Schottky diode characteristics. For the first time, electrical measurement was complemented with mechanical adhesion testing and demonstrated that Ni is a suitable contact metallization for high power, high temperature and good mechanical strength diamond Schottky barrier diode applications.

[1] Umezawa, H., Kato, Y. & Shikata, S. 1 ohm On-Resistance Diamond Vertical-Schottky Barrier Diode Operated at 250°C. Appl. Phys. Express 6, 011302 (2013).

Gallium nitride (GaN) becomes more and more popular for power applications. Using heterostructures for carrier confinement allows offering high electron mobility and consequently, to achieve very low on-resistance devices.

In ToPoGaN1 project, the main technological process steps were validated, allowing the realization of functional AlGaN/GaN HEMTs on 150 mm silicon substrates. These devices exhibited breakdown voltages well above the targeted 600 V value (Figure 1) and specific on-state resistance of 2.5mΩ.cm^2.

Unfortunately, HEMTs are normally-on devices whereas normally-off ones are preferred for power applications, since it simplifies the design of driving circuits. To address this problem, new architectures of normally-off AlGaN/GaN HEMTs were recently proposed [*MAI13369*] and patented [*BR1303*], thanks to a preliminary 2D TCAD study. Furthermore, GaN MOS capacitances were realized: after the study of different interfacial treatments and dielectric (SiO_2) deposition on GaN, an optimal process was issued and resulted in minimized interface trap densities (close to 10^{10} cm^{-2}.eV^{-1}) [*RVSI11330*] [*[TH11451*].

For the characterization needs of wide bandgap devices, we developed a specific high-voltage (≤ 3kV) test bench for wafer-level measurement. For its implementation, we designed a circuit dedicated to energy switching measurement. To accurately estimate switching losses of fast power wide bandgap devices, chosen technique is based on the opposition method that does not involve direct transistor current measurement therefore not disturbing the switching behavior of the transistor under test (Figure 2).

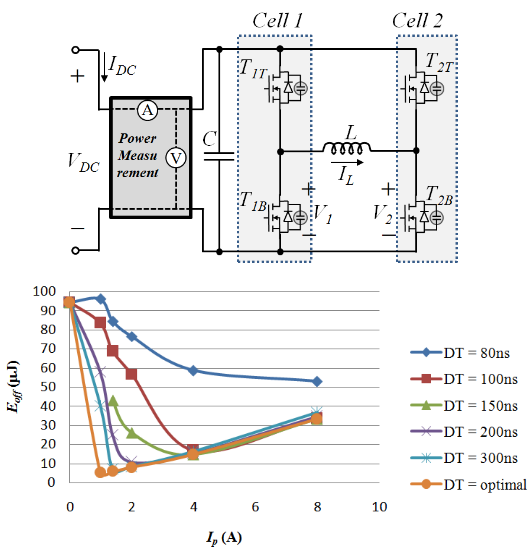

Figure 2: Proposed circuit for the measurement of energy switching (top) and example of measurement data for a commercial SiC MOSFET device.

2.1.3 Power Integration

For medium power applications (current densities of about 100 A/cm^2 and V_{BR} ≤ 1200 V), we work on both technological and design solutions for the development of monolithic multi-switches silicon chips to enable customizable power systems in the same way as ASIC does in the digital world.

The originality of the concept that was patented [*BR1108*], is to integrate an array of high-side power switches in a single die (common anode on Figure 3) and to do the same for low-side switches (common cathode). The advantages of this integration approach that could be called "Power ASIC" are twofold: improvement of electrical performance as well as reliability of the power module.

To this aim, the proposed Power ASIC chip is composed of multiple vertical Reverse Conducting IGBT (RC-IGBT) power switches that share the same lightly doped N$^-$ region. Using our flexible IGBT process, this innovative concept was implemented on silicon for the case of a three poles monolithic chip called "common anode" chip (Figure 3).

Moreover, using the same process, we realized and experimentally validated the operating modes of an RC-IGBT structure [*MAI13285*] [*RVSI13693*] [*[TH14239*]. We are currently working on the development of a specific P$^+$ wall technological step for its integration in our flexible IGBT process. This isolation step is essential to experimentally validate the multi-switches chip called "common-cathode".

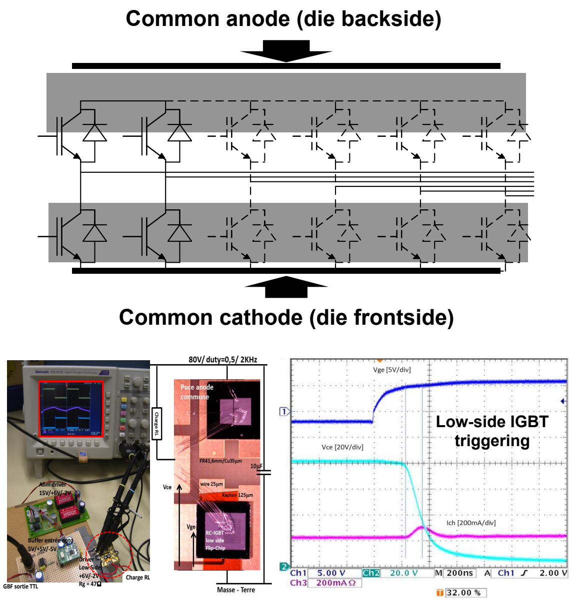

Figure 3: Schematic illustration of "Power ASIC" concept (top) and experimental validation of a functional H-bridge.

2.1.4 Energy Conversion Architecture

Within the framework of LISPA Freescale-LAAS joint lab (2005-2008), we developed and experimentally validated the concept of multi-phase and interleaving step-up and step-down DC-DC converters (1V, 1-4MHz, 150A) for embedded applications (from phone, laptop to computers) with high efficiencies over a wide range. In cooperation with TOTAL Company, this concept was applied to photovoltaic (PV) energy power conversion to improve efficiency and reduce stress in active and passive components, then resulting in lifetime increase of the global power system [*[TH13266*]. This work was awarded the *Best Paper and Best Oral Presentation* at the 38th Annual Conference of IEEE Industrial Electronics (IECON 2012) in Montreal (CA) [*MAI12516*]. These studies resulted in two international patents

[*BR0911*] [*BR0912*] in collaboration with URV University in Spain [*RVSI14192*], [*RVSI12660*].

Furthermore, we developed a high expertise in efficient PV energy production even in shadowed (Figure 4) or aging modules, proving each year that the dream concept of one converter including its MPPT for a small group of PV cells will drastically improve the energy production. We developed MPPT control laws based on extremal control that are at the same level as the state-of-the-art ones designed by American research teams, achieving a static efficiency better than 99.4 % and over 96 % in transient mode .

A new concept of electronic management system was designed to optimize matching during the global lifetime of the PV system. It is based on new distributed architectures, arranged as independent modular ones which are only used in optimal power transfer and can be disconnected by a dedicated control management if a default occurs. This work was initiated with a first patent [2] filed in 2008 and additional improvements were recently proposed and protected by a second patent [*BR1302*] [[*TH13269*]. These distributed architectures require new low-power integrated circuits and functions.

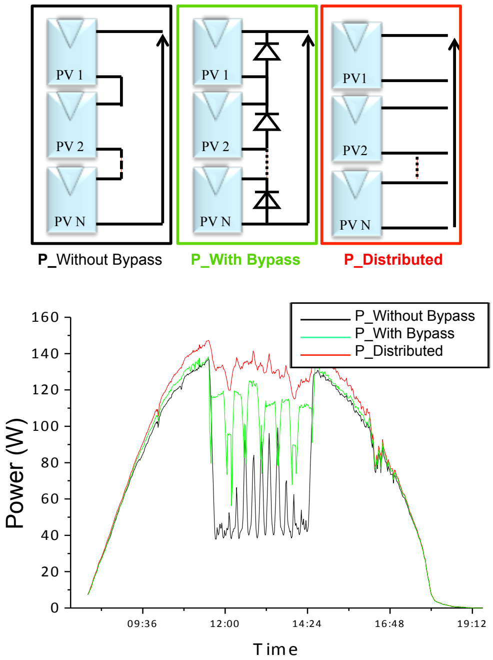

Figure 4: Different types of PV architecture (top) and experimental comparison of resulting output power in shadowing conditions.

When using renewable energies such as the photovoltaic one, an important issue is the management of intermittence that requires efficient storage solutions. Within ANR LiPV project and the PhD work of Jean-François Reynaud [[*TH11004*], we have proposed and experimentally validated various architectures for innovative PV modules integrating lithium batteries and their associated battery management system (BMS). This PhD study was awarded the Doc'innov price by the Doctoral council of the University of Toulouse. For the experimental validation of management algorithms and the qualification of conversion chains, a specific test bench was developed [*MAI10337*].

2.2 Robustness And Reliability

Taking into account the requirements for robustness and reliability of a device or a system at an early stage of the design is essential. It is even more essential in the field of power electronics where in addition to environment constraints the system can undergo harsh functional operation conditions (high voltage, high current, high electric field).

In GE Theme, we have focused our activities on improving the robustness of power devices under Natural Radiative Environment, ESD protection strategies and predictive multi-physics modeling.

2.2.1 Radiation Hardening

Electronic systems embedded in aeronautics and space applications are subjected to severe constraints of Natural Radiative Environment (NRE). Electrical energy management systems use power components such as VDMOSFETs, IGBTs and SuperJunction devices, which are particularly sensitive to NRE particles. In order to propose radiation-hardening solutions at component and/or system level, we have studied and compared the various involved physical mechanisms in advanced power devices in radiative environment using 2D and 3D TCAD simulations. Three PhD theses [[TH09913] [[TH13401] [[TH13823] were defended that allowed defining a simulation methodology with a good correlation to experiments based on laser testing and heavy ions. Several original design and technological solutions were also proposed for power structures hardening [*RVSI12621*] [*RVSI14204*].

2.2.2 ESD Protection Strategies

To tackle the pressing challenges of the ESD protection of advanced CMOS and smart power technologies, we established strong and fruitful cooperation with industrial partners (Freescale, STMicroelectronics, ON Semiconductor). The motto is high efficiency both in terms of silicon area and robustness level. Concurrently, we also carried out more prospective studies on the protection of MEMS devices and on integrated ZnO-based varistors.

To provide efficient ESD protection to advanced technology nodes (45nm and 32nm), in partnership with STMicroelectronics, we have studied SCR-based structures to significantly improve the robustness of these technologies. Main result is an innovative global protection strategy based on a network of 3 bi-directional SCR, called « Beta Matrice ». On a CMOS 32nm technology, it resulted in 2kV HBM robustness with a reduced silicon footprint [RVSI10273] [[*TH11396*].

We also initiated an original activity on the effects of high temperature on the ESD robustness of smart power technologies that allowed proposing an innovative solution to improve both robustness and temperature behavior of ESD protections. Proposed solution

[2] M. Vermeersch, B. Estibals, C.Alonso, Electronic management system for photovoltaic cells, Patent n° WO2010070621, Filed 18/12/08, Published 24/06/10.

combines in the same device a MOS (for fast triggering), and an IGBT as well as an SCR (for its better temperature behavior and lower on-resistance). This resulted in dividing by 10 the silicon area of the ESD power clamp together with drastically improving the robustness from 2kV to 8kV HBM. Original solutions (reduced MOS channel) have been implemented to control the SCR triggering. This latter solution has also an interest for providing improved radiation hardening to an IGBT device [RVSI13419] [*[TH12329*].

A pioneering work was also achieved on the ESD reliability of MEMS in cooperation with MINC team within the framework of AMICOM European Network of Excellence. The studied device was a 40GHz MEMS RF capacitive switch. Two major results were highlighted. Firstly, the MEMS ESD robustness is extremely low (under 100V) and some external protections are needed. Secondly, an innovative method for accelerated testing of capacitive MEMS have been proposed [RVSI12049].

Finally, we are carrying out a long running and very high-risk but exciting project whose ambitious objective is the on-chip (or above IC) integration of varistors based on zinc oxide (ZnO) material. We recently achieved and demonstrated the first functional integrated varistor on silicon wafer using inkjet printing technique (Figure 5). It exhibits an excellent robustness for a high voltage clamping device: higher than 4 mA/µm, 0.4mA/µm^3 for 100ns current pulse with a maximum current density higher than 400 kA/cm^2 and limited leakage current of 50µA at 40V. This multidisciplinary project involves three different laboratories in Toulouse (CEMES, LGC and LAAS). This first important breakthrough paves the way for future studies and developments.

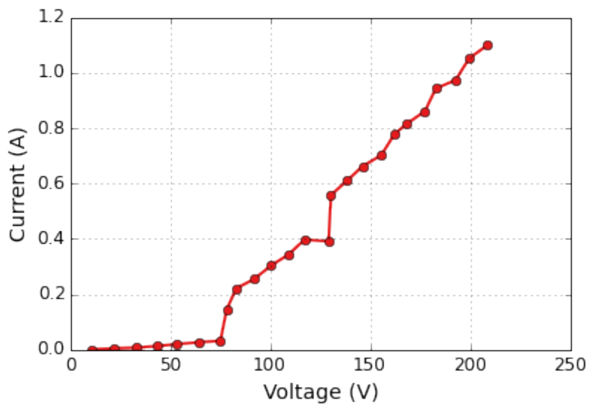

Figure 5: First proof of concept of ZnO-based integrated varistor. 250µm-width device electrical characteristic under 100ns-pulse IV characterization.

2.2.3 Predictive Multi-Physics Modeling

Electro-thermal-mechanical modeling. Electro-thermal-mechanical modeling was carried out within the framework of an inter-Carnot ANR project "ReMaPoDe (Reliability Management of Power Devices)". The overall project objective was to provide a sensing device that could assess the real-time ageing status of a power assembly by monitoring its thermal and mechanical states during operation.

This work [*[TH12444*] mainly consisted in highlighting the relationship between the assembly mechanical ageing and the observed electrical evolution. Moreover, given the thermal issues related to embedded applications, the electrical characteristics identified as an ageing indicator should allow overcoming the detrimental effects of temperature. Consequently, after a thorough analysis of the different ageing and failure mechanisms encountered in power assemblies, we have identified relevant electrical characteristics that are promising for real-time monitoring of the mechanical ageing status of a power device assembly despite ambient temperature variations and assembly material ageing [*RVSI14032*].

With respect to thermo-mechanical strain modeling, an efficient simulation methodology permitting simultaneous computation of distributed electrical and thermal modeling has been developed. This is especially suited to model hot spot emergence and local electro-thermal runaway phenomenon [*RVSI11578*] [*RVSI11204*] [*[TH13358*].

Electromagnetic compatibility (EMC). Between 2010 and 2013, several important breakthroughs have been achieved.

A pioneering work about the impact of ageing of ICs on the long-term EMC has been initiated (EMRIC ANR JC project). For the first time, we have demonstrated by several experimental and modeling studies that the IC aging (accelerated in nanoscale technologies and in harsh environment) can induce non-negligible drifts of electromagnetic emission (EME) and/or electromagnetic susceptibility (EMS) levels (Figure 6). The evaluation of the non-compliance risks can be done either by adapted qualification tests (EMC tests on aged samples) or by EMC modeling which integrates the ageing factor.

We have started to build up equivalent electrical models for this purpose. All the results have been published in numerous articles and presented in several international workshops about EMC and reliability [RVSI13690] [RVSI14018] [*[TH11897*], some of them as invited presentations. Part of these studies obtained the best paper award at EMC COMPO 2013 in Nara (Japan) [MAI13692].

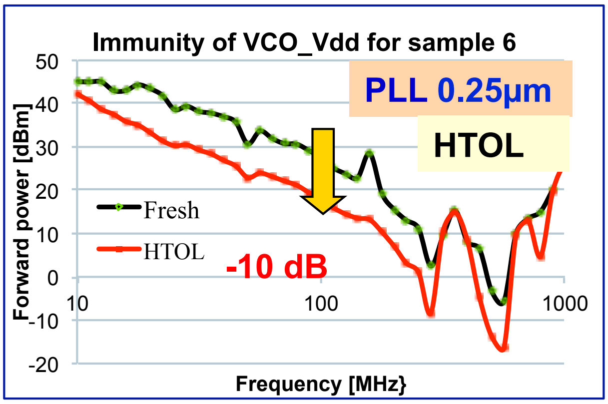

Figure 6: Impact of ageing on measured EMI immunity of a VCO circuit that was submitted to High-Temperature Operating Life (HTOL) tests.

For the first time, we used on-chip sensors to characterize electrical signals induced in an IC during conducted susceptibility tests, with a good time resolution (10 ps) [*RVSI12305*]. These experimental results have shown the strong influence of IC interconnects on the coupling of electromagnetic interferences and, thus, their importance in the modeling of IC susceptibility. This preliminary work has initiated our participation to European AUTOMICS project, focused on the modeling of substrate coupling issues in automotive circuits.

An on-chip sensor has also been integrated in a test chip (Milady) developed in collaboration with Freescale Semiconductor, within E-Mata-Hari project. This circuit is dedicated to the characterization and the modeling of miniature injection near-field probes developed by our team and other partners. The main application of this study is cryptographic attacks.

This on-chip sensor was also successfully adapted for monitoring the ESD current paths within a powered IC when submitted to an ESD stress [RVSI13700].

Electrostatic Discharges (ESD). Regarding system level ESD, the main challenge consists in developing efficient and accurate predictive simulation methodologies. On this topic, in partnership with industrial partners, namely FREESCALE, VALEO and On Semiconductor, 2 PhD theses were carried out and defended [*[TH11906*] [*[TH13270*]. We developed new investigations techniques that allow, on the one hand, injecting well-defined ESD stresses (like TLP or double pulse TLP) and on the other hand, providing accurate techniques to characterize real ESD stress propagation and waveform at PCB level but also at chip level [RVSI13689].

In parallel, we proposed and experimentally validated a behavioral modeling approach to predict functional and hard failure [RVSI10099]. Since 2009, LAAS (F. Caignet) has also been involved in the international ESDA standard committee related to system level ESD, and is leading a discussion group whose objective is the writing of a white paper on parameters extraction for system level ESD modeling.

Characterization methods are essential for modeling validation. In particular, we carried out an original study on a new transient TLP (T-TLP) setup that allows characterizing the ESD protection behavior within the sub nanoseconds of the ESD stress and then detecting excessive overshoots. With this measurement technique, we showed that some ESD protections exhibit important over-voltages during the turn-on phase, which can have catastrophic impact on the protected circuit. Concurrently used with TCAD simulations, this tool was applied to the optimization of ESD protection devices for smart power technologies [MAI13792] [*[TH12410*].

Regarding TLP techniques, we initiated a worldwide network (France, Belgium, USA, Japan) aimed at developing open-source software dedicated to the analysis of such measurement results (import of different setup results, graphical comparison…). LAAS wrote about 95% of software codebase. There were also important contributions from all main commercial-setup vendors to write import's code from their proprietary format. The latest version of this software was downloaded more than 700 times http://code.google.com/p/esdanalysistools/downloads/list.

2.3 Energy Autonomy Of Embedded Systems

The development of low-power integrated circuits (such as sensors, microprocessors or wireless communication chips) has made embedded systems increasingly popular. These systems are meant to operate in controlled/uncontrolled environments, gathering, processing, storing and communicating information wireless. In order to supply efficiently and continuously the power to these systems, an attractive solution is to combine energy harvesting (thermal, vibrational or solar energy) with an energy-storage micro-device.

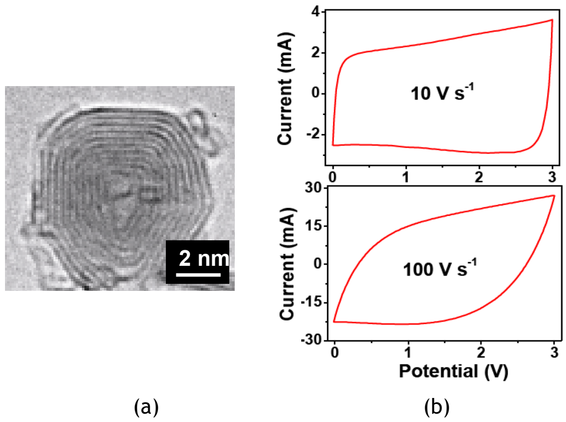

Figure 7: Carbon onion based micro-supercapacitors: view of a carbon onion (a) and cyclic voltammograms (CVs) of at different scan rates.

On-chip micro-supercapacitors show very interesting characteristics when it comes to these applications, because of their extended lifetime and high power density. Given our expertise in the field of power integration, and in cooperation with CIRIMAT laboratory, we have chosen to start a new field of research aiming at developing these on-chip micro-supercapacitors.

Concurrently, in cooperation with different teams at LAAS (MINC, N2IS) and partners in the field of aerospace (Airbus, CNES, Thalès Alenia Space), we have initiated a research activity related to the energy autonomy of wireless sensors in harsh environment. To tackle this challenge, we have focused our studies on battery-free systems and are working on the efficiency of energy management circuits, on storage methods using supercapacitors, and on the implementation of energy transducers: photovoltaics, thermoelectricity, and in the long term aeroacoustic.

2.3.1 Microstorage

The challenges of on-chip microstorage are related to the integration of an active material (generally carbon-based) and an electrolyte on silicon. This includes nanostructuration techniques, cost-effective deposition methods and hermetic packaging [*BR1007*]. To this aim, we have developed different IC-compatible technological processes (inkjet printing [*RVSI09320*], screen-printing [*RVSI11646*], electrophoretic [*RVSI10534*] and electrolytic [*RVSI13016*] deposition, thin film processing [*RVSI12608*]) to integrate various innovative materials (activated carbon, carbon onions, carbide derived carbon, carbon nanotubes, carbon nanowalls, RuO_2…) for the development of enhanced micro-supercapacitors. Specific capacitances up to 675 mF/cm^2 were obtained with carbon nanowalls and components with extremely high power densities (700 mW/cm^2) using carbon onions (Figure 7) were realized.

Most of micro-supercapacitors are nevertheless based on liquid electrolytes (aqueous or organic), which can be a major problem when it comes to the realization of functional components using the silicon micro-fabrication technology. We are therefore currently investigating all-solid-state micro-supercapacitor based on innovative solid electrolytes.

Figure 8: A321 left wing implementation of the wireless sensors together with the battery-free power supply based on solar energy harvesting and storage on supercapacitors.

2.3.2 Energy Harvesting And Power Management Of Battery-Free Wireless Sensor

Over this period, this new activity has significantly developed with the recruitment of an assistant professor, and through one project funded by the "Investissements d'avenir" within CORAC program and one European CHIST-ERA project as coordinator.

First results had been initially obtained within the framework of SACER FUI project and AUTOSENS FNRAE project. The main challenge of SACER, dedicated to aeronautic in-flight tests, was to provide 3W energy autonomy to a real-time wireless sensor network. To this aim, we proposed a battery-free architecture based on supercapacitors, solar energy harvesting and appropriate power management including MPPT and startup techniques [*RVSI11665*] [*RVSI13440*] [*[TH10797*]. The results of this project are currently being transferred through a bilateral relationship with Airbus Group (in-flight tests department) and a first successful flight was realized in June 2014 (Figure 8).

Within AUTOSENS project dedicated to Aircraft Health Monitoring (AHM), we proposed an original multisource battery-free architecture using transient thermal gradients (during climb and descent) as a primary source and permanent mechanical vibration as a secondary source. To increase the efficiency of the transient thermogeneration, the thermoelectric transducer was coupled to a capsule with a phase change material (water) [*RVSI13300*]. A dedicated low-power multi-source power converter was designed and successfully tested[3] exhibiting a very low quiescent current of 300 nA and a maximum efficiency of 82% that is within the performance of proposed LDO regulators of the state-of-the art[4].

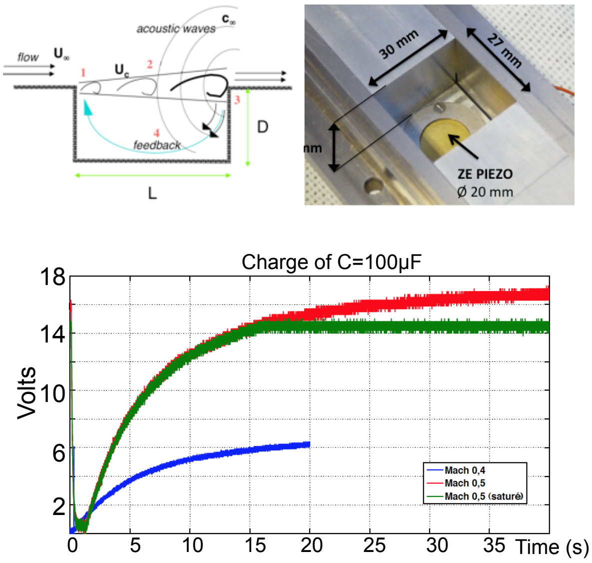

Figure 9: Aeroacoustic energy harvesting principle and implementation (top) and resulting harvested energy on a capacitive load as obtained in a wind tunnel.

In the field of energy capture, we carry out a more prospective work on the capabilities of aeroacoustic energy harvesting. This work was co-funded by DGA and Intesens and continues within CORALIE project (Investissements d'avenir). We have demonstrated the possibility of powering an electronic system by the mechanical energy generated by the noise created on purpose by disrupting the laminar flow of an aircraft aerodynamic surface (Figure 9) [*MAI12610*]. On this topic, we are collaborating with ONERA and IMFT labs.

We have also proposed a novel adaptive topology to optimize the dynamic performance of supercapacitors used to store energy that will be integrated within the framework of CHIST-ERA SMARTER project in cooperation with the University of Barcelona and the University of Exeter [*MAI12609*].

2.4 Tools and Demonstrators

For the needs of our research studies, several original tools, in the field of characterization, software and modeling were developed. Another important step for the validation of innovative research concepts is the realization of demonstrators. They are both summarized in Table 2.

[3] C. Vankecke, L. Assouère, A. Wang, P. Durand-Estèbe, F. Caignet, J.-M. Dilhac, M. Bafleur, Multisource and Battery-free Energy Harvesting Architecture for Aeronautics Applications, Power Electronics, IEEE Transactions on, Vol. PP, Issue: 99, June 2014.

[4] J. Colomer-Farrarons, P. Miribel-Català, A. Saiz-Vela, and J. Samitier, "A Multiharvested Self-Powered System in a Low-Voltage Low-Power Technology," IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 4250-4263, Sept. 2011.

HV-CARAC and **DIAMOND_design** tools were motivated by the new research activities related to wide bandgap power devices. **ADREAM_NRJ** concerns the photovoltaic platform of ADREAM building and the related characterization test benches for assessing either new photovoltaic solar cells or new converter architectures in real conditions. **Near-field scan** and **Satellite/Thunderstorm** are related to electromagnetic compatibility and electrostatic discharges (ESD) research issues. It has to be noticed that the listed demonstrators successfully validated a full function: powering of a wireless sensor, one of them was embarked for flight tests onboard an Airbus A321 and the realization of a functional H-bridge using monolithic integration on silicon (Power ASIC).

Table 2: Tools and Demonstrators

Acronym	Description
HV-CARAC	High-voltage devices (> 1 kV) characterization platform.
ADREAM_NRJ	Photovoltaic platform and related characterization test benches.
DIAMOND_design	TCAD platform for diamond devices design.
Near-field scan	Near-field scan test bench.
SATELLITE/[THUNDERSTORM	Software tool : ThunderStrom is a python library to manipulate ElectroStatic Discharges (ESD) measurement-setups data.ThunderStorm is heavily used by Satellite (http://esdanalysistools.github.io/Satellite/).
FLYING_NRJ_HARVESTER	Demonstrator: Autonomous battery-free photovoltaic system for sensor powering during flight test.
SDS	Demonstrator: Wireless battery-free system (thermal energy harvesting, sensing & communication) for the monitoring of hatch opening in an airliner.
Aeroacoustic harvesting	Demonstrator: Aeroacoustic energy harvesting battery-free system for data logger powering.
Power ASIC	Demonstrator: Functional integration on silicon of (≤1200V) multi-switches.

3 Main Publications

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[TH10371] B.BERNOUX, Caractérisation de MOSFETs de puissance cyclés en avalanche pour des applications automobiles micro-hybrides INSA de Toulouse, 31 Mars 2010, 147p.

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[TH10797] D.MEEKHUN, Réalisation d'un système de conversion et de gestion de l'énergie d'un système photovoltaïque pour l'alimentation des réseaux de capteurs sans fil autonome pour l'application aéronautique. Institut National des Sciences Appliquées, Toulouse, 19 Novembre 2010, 197p.

[TH10819] J.LE GAL, Intégration des fonctions de protection avec les dispositifs IGBT. Université Paul Sabatier, Toulouse, 20 Avril 2010, 123p.

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[TH11464] H.DIA, Contribution à la modélisation électrothermique: Elaboration d'un modèle électrique thermosensible du transistor MOSFET de puissance. Institut National des Sciences Appliquées, Toulouse, 12 Juillet 2011, 183p.

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