IRT SAINT EXUPÉRY

Fonctionnement collaboratif entre l'IRT St Exupéry et la plateforme PROOF

COS – PROOF 05.10.2022

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www.irt-saintexupery.com

Reminder

12 competences

High voltage energy >

High Reliability Energy >

High density energy >

Metallic materials and processes >

Surfaces / assemblies >

Composite materials >

Advanced Learning >

AI for critical systems >

Autonomous Connectivity & Detection >

Systems Engineering >

Multi Discipline Optimization >

Critical Embedded Systems >

4 Technological Axes

Greener Technologies

Advanced Manufacturing Technologies

Smart Technologies

Methods and tools for the development of complex systems

- Improve products life cycle
- Enable increased electrification of systems
- Reduce products weight and volume

Electrification

of (embedded) systems and functions !

FRENCH
INSTITUTES OF
TECHNOLOGY

Technological & Methodological Levers

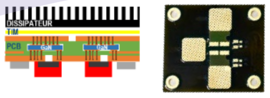
The big picture

SAINT EXUPÉRY IRT

Optimized Control

Laplace

WBG Power Module Integration



WBG PCB embedded

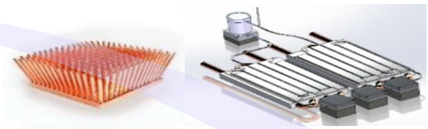
DGA

ims

CPES

Primes

LAAS CNRS

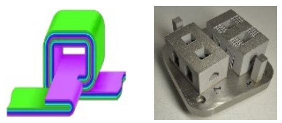


Cooling Systems

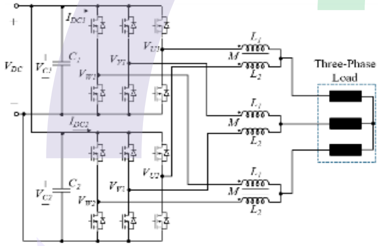
icam

LAAS CNRS

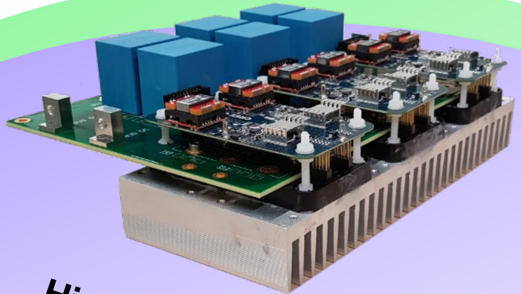
Laplace



Magnetics and bobins

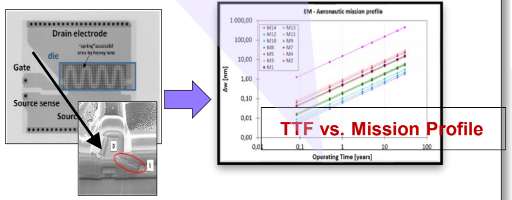


Converter Topology



High Integration & Efficiency

High Dependability (harsh Envir / High constrain)



TTF vs. Mission Profile

Failure Risk Assessment Methodology

ISEN ALL IS DIGITAL!

SuperGrid Institute

Ampère

LAAS CNRS

ceatech

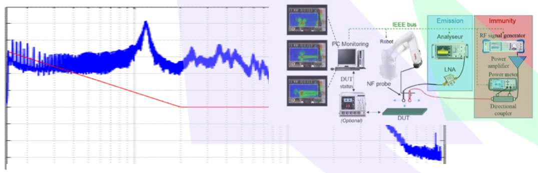
DGA

INSTITUT VEDECOM

cnes CENTRE NATIONAL D'ÉTUDES SPATIALES

Laplace

SATIE



EMC, EMI from component to system
(active filter, Near field Scanning, …)

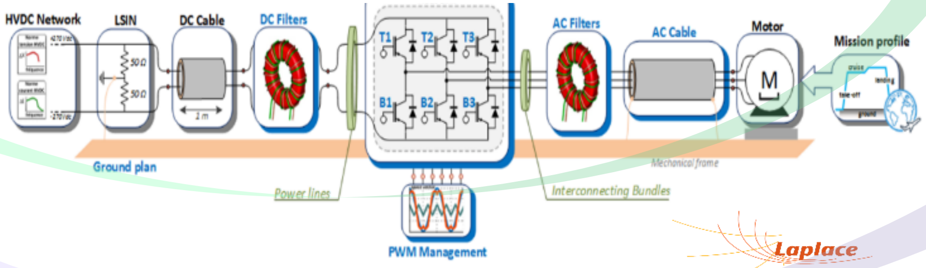
IETR

LAAS CNRS

SATIE

ims BORDEAUX

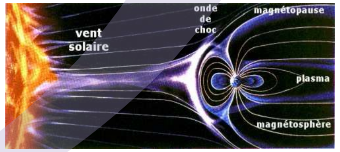
Multidisciplinary Design Optimization



Laplace

In-System-Validation

Testing and Optimizing the converter in the entire EM chain



Cosmic radiation Immunity

NANOELEC

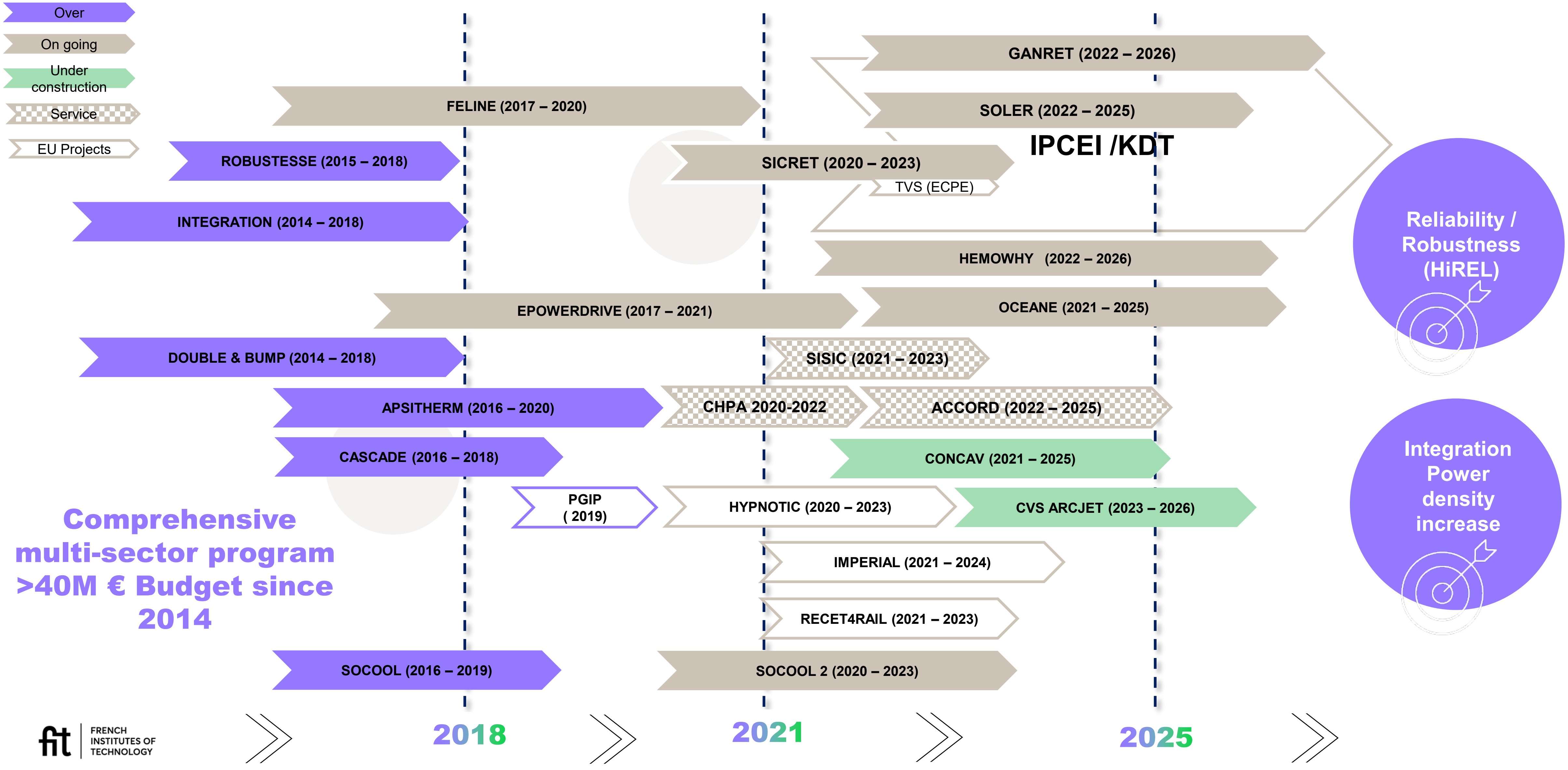
ESRF The European Synchrotron

cnes CENTRE NATIONAL D'ÉTUDES SPATIALES

CERN

ies l'institut d'électronique

Dependable Electronics for Embedded Systems:
Projects supporting roadmap



Over

On going

Under construction

Service

EU Projects

GANRET (2022 – 2026)

FELINE (2017 – 2020)

SOLER (2022 – 2025)

IPCEI /KDT

ROBUSTESSE (2015 – 2018)

SICRET (2020 – 2023)

TVS (ECPE)

INTEGRATION (2014 – 2018)

HEMOWHY (2022 – 2026)

EPOWERDRIVE (2017 – 2021)

OCEANE (2021 – 2025)

DOUBLE & BUMP (2014 – 2018)

SISIC (2021 – 2023)

APSITHERM (2016 – 2020)

CHPA 2020-2022

ACCORD (2022 – 2025)

CASCADE (2016 – 2018)

CONCAV (2021 – 2025)

PGIP
(2019)

HYPNOTIC (2020 – 2023)

CVS ARCJET (2023 – 2026)

IMPERIAL (2021 – 2024)

RECET4RAIL (2021 – 2023)

SOCOOL (2016 – 2019)

SOCOOL 2 (2020 – 2023)

Reliability / Robustness (HiREL)

Integration Power density increase

Comprehensive multi-sector program >40M € Budget since 2014

2018

2021

2025

FRENCH INSTITUTES OF TECHNOLOGY

FELINE : Fiabilité ÉLectronique INtégréE

Centre Français Fiabilité

- **13** Industriels
- **4** PMEs
- **5** PhD (4 Labs)
- **3** Collaborations
- **>15** Publications and Industrial Reports

OBJECTIVES

- Develop and apply the Failure Risk Assessment Methodology (FRAME) to COTS components (DSM and WBG) in real operational environments (Mission Profile)
- Address component obsolescence from an EMC perspective through the use of digital simulations
- Durability of electronic component assemblies in small signal applications

6,9 M€

48 Mois (2017– 2021)

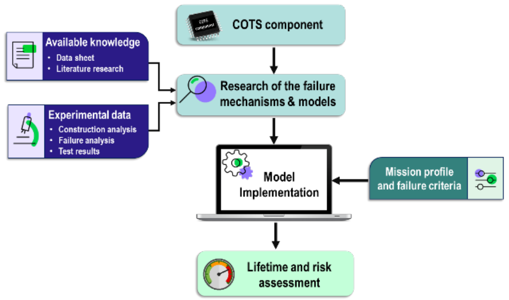
ACTIA, AIRBUS, AIRBUS DS, CONTINENTAL, ELEMCA, NEXIO, LIEBHERR, SAFRAN TECH, TECHFORM, THALES AV, THALES AS, TRAD, ZODIAC AEROSPACE

LAAS-CNRS, INSA Toulouse, IMS Bordeaux, IETR-CNRS, IES-CNRS

Lot 1

Reliability of COTS (DSM and WBG)

- PoF modeling of DSM and WBG technologies: TDDB, BTI, HCI, EM…
- Deployment of the FRAME approach
- Reliability platform (tool): agile and easy to use.



COTS component

Available knowledge
- Data sheet
- Literature research

Experimental data
- Construction analysis
- Failure analysis
- Test results

Research of the failure mechanisms & models

Model Implementation

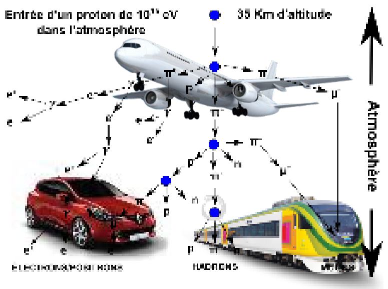
Mission profile and failure criteria

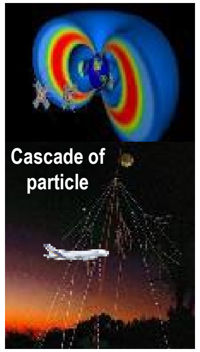
Lifetime and risk assessment

Lot 2

Radiation

- Behavior of recent semiconductor technologies with respect to cosmic and atmospheric radiations: Heavy ions, Neutron, Proton and TID.

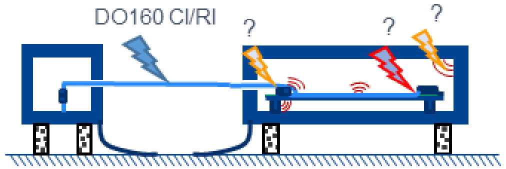




Lot 3

CEM

- Validate the non-regression of the EMC performance of an equipment to cope with the change of a component using measurement on a component / electronic board:
  - ✓ Near field emission measurement (NFSe),
  - ✓ Near field immunity measurement (NFSi).

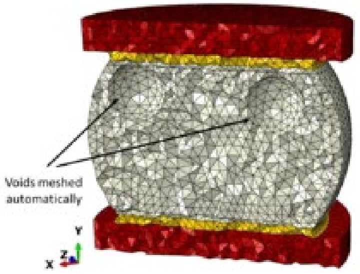


How to decline EMC constraints (DO160/CISPR) at Board or Component level?

Lot 4

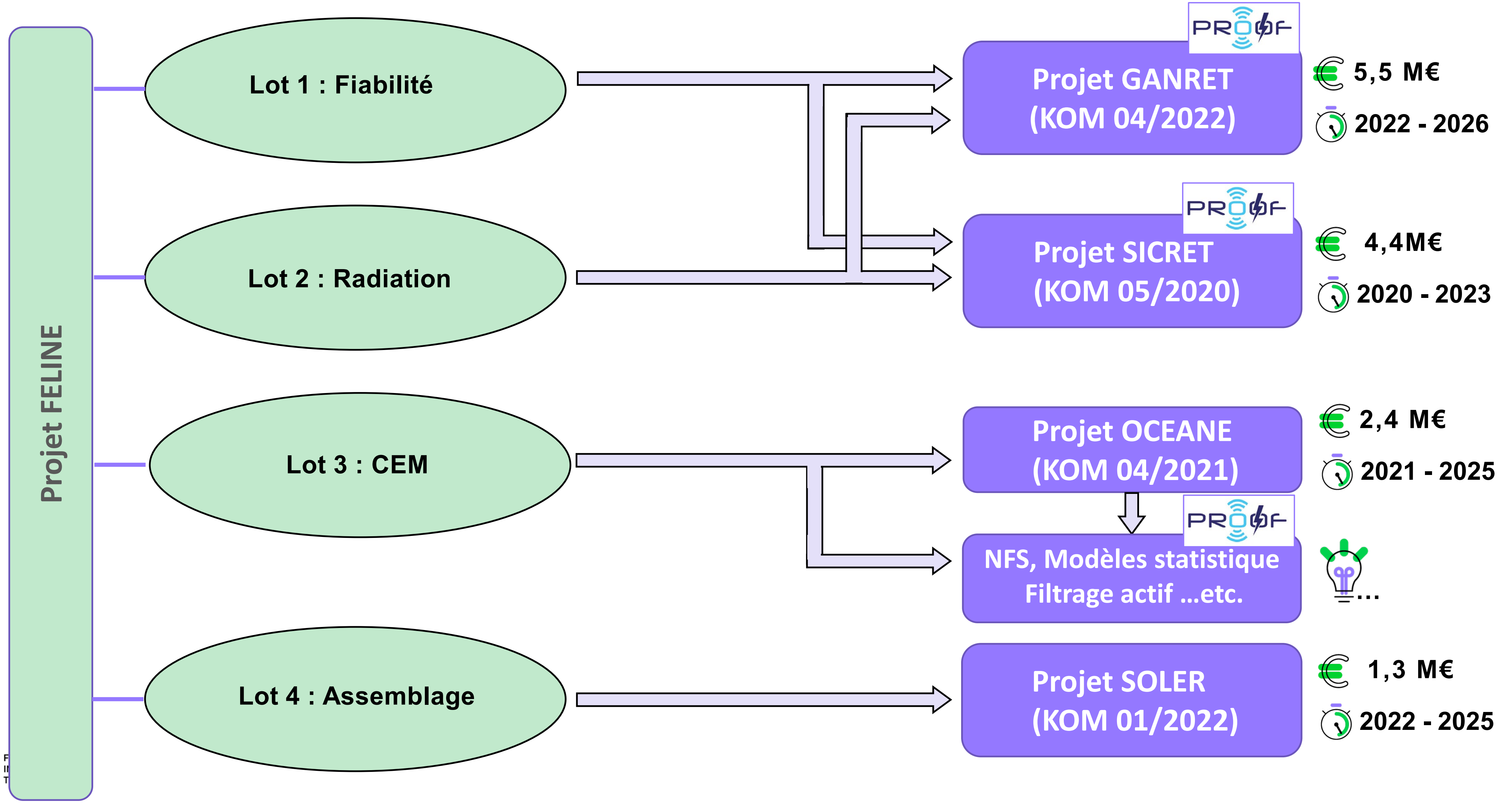
Electronic assemblies

- Durability of low power electronic boards: mechanical fatigue of microelectronic assemblies
- Multi-scale modeling: from the solder joint to the equipped board.



Organisé par :

Après FELINE



Projet FELINE

Lot 1 : Fiabilité

Lot 2 : Radiation

Lot 3 : CEM

Lot 4 : Assemblage

Projet GANRET (KOM 04/2022)
5,5 M€
2022 - 2026

Projet SICRET (KOM 05/2020)
4,4M€
2020 - 2023

Projet OCEANE (KOM 04/2021)
2,4 M€
2021 - 2025

NFS, Modèles statistique Filtrage actif …etc.
…

Projet SOLER (KOM 01/2022)
1,3 M€
2022 - 2025

GaNRET

GaN (Power Transistor) Reliability Evaluation for Transport

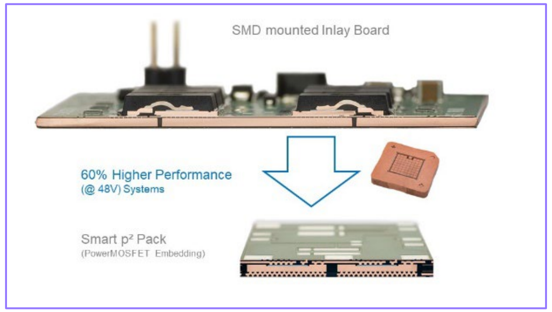
Project Set-up Team:

cea | fit FRENCH INSTITUTES OF TECHNOLOGY [VEDECOM | IRT SAINT EXUPERY | NANOELEC]

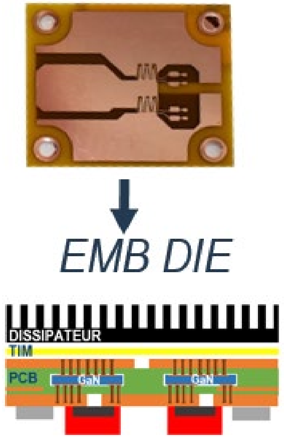
TENTATIVE: BUDGET: ~ **10 M€ -** DURATION: **48MM** Start Date: **2022-Q1**

❖ Main Challenges:

- PoF not-well understood / established
- Panoply of (not mature) technologies (e/d mode)
- Design rules and test protocol for advanced (**embedded**) packaging

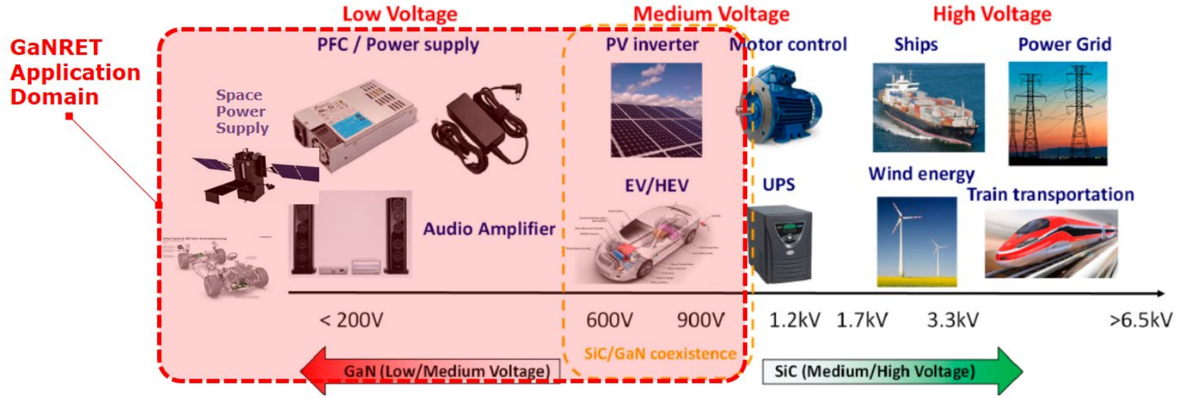


Source: Schweizer and Infineon

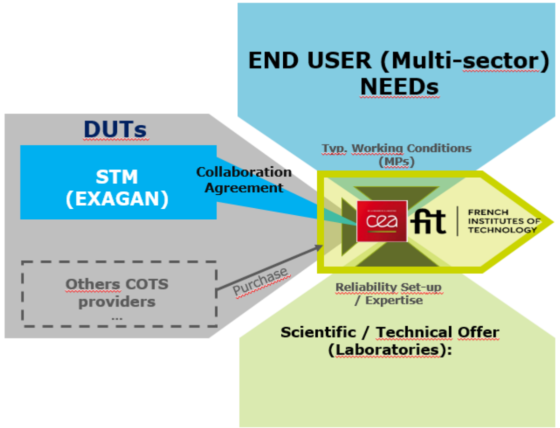


Source: IRT- EPOWERDRIVE Project

❖ Application domain:



❖ Project Rational:



i) **Reliability analysis** (advance in the understanding of underlighying failure mechanisms)

ii) **Definition of test procedures** and methodologies adapted to user mission profiles → toward dedicated GaN technology qualification

iii) **Establishment of mitigation solution** such as design recommendation (e.g. SoA, Derating rules for safety margins, …)

afnor
IEC
AEC-Q
JEDEC
ECPE

GANRET An end-user driven project

Gallium **N**itride **Re**liability for **T**ransport

> 5.5M€

48 months
Start: 15.03.2022

16 partners

Context:

GaN HEMT are the ideal candidates for **high-power** & **high-frequency** applications

increased <u>power density</u> &
improved <u>efficiency</u>

Challenge& Motivation:

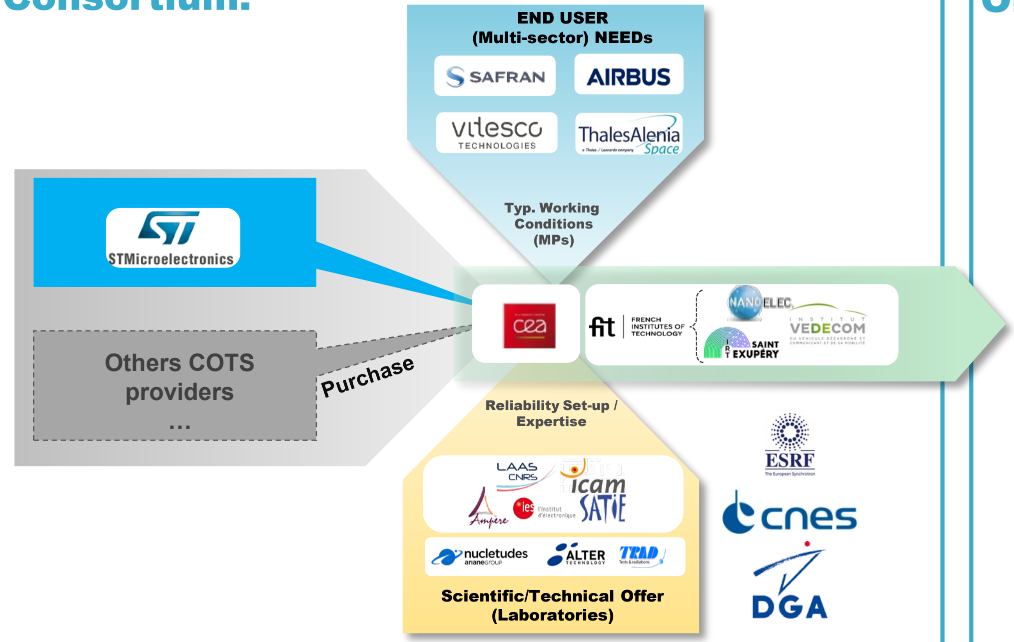
- ☐ GaN technology maturity shortcoming
- ☐ Panoply of technologies & providers
- ☐ Lack of suitable qualification standards

<u>Reliability</u>
- Qualification
- Robustness
- Durability

<u>Main objective:</u>

Enabling GaN based power electronics insertion into **severe** environmental constrains

Consortium:



END USER
(Multi-sector) NEEDs

Typ. Working Conditions (MPs)

Others COTS providers
…

Purchase

Reliability Set-up / Expertise

Scientific/Technical Offer (Laboratories)

Objectives Implementation:

Understanding of underlying PoF: Identification of the **critical stressors and indicators** specific to the given usage mission profile

Test-for-GaN: Definition of test **methodologies adapted to GaN** technology and support the definition of dedicated **qualification protocols**

Design-for-GaN: Definition of **margin aware design rules** and methodology for **risk assessment** and mitigation (design recommendation, safety margins, etc.)

Manufacturing-for-GaN: Support GaN ODM to **improve manufacturing** technology maturity ⇨ Technology improvement

AEC-Q
afnor
ECPE
IEC
JEDEC

WP1
DUT & Mission Profile Specification

Market analysis
DUTs selection
Mission profile analysis

WP2
Electrical Characterization & Modelling

Measurement protocol
Electrical characterization
Thermal investigation

WP3
Reliability Investigation

Static aging tests
Dynamic aging test
Short-circuit

WP4
Radiation Immunity Assessment

Alternative test methodologies
NDT methodology development
Mutual effect reliability-radiation

WP5
Exploitation & Capitalization

Reliability tool for risk assessment
Lighthouse initiatives
Supporting standardization entities

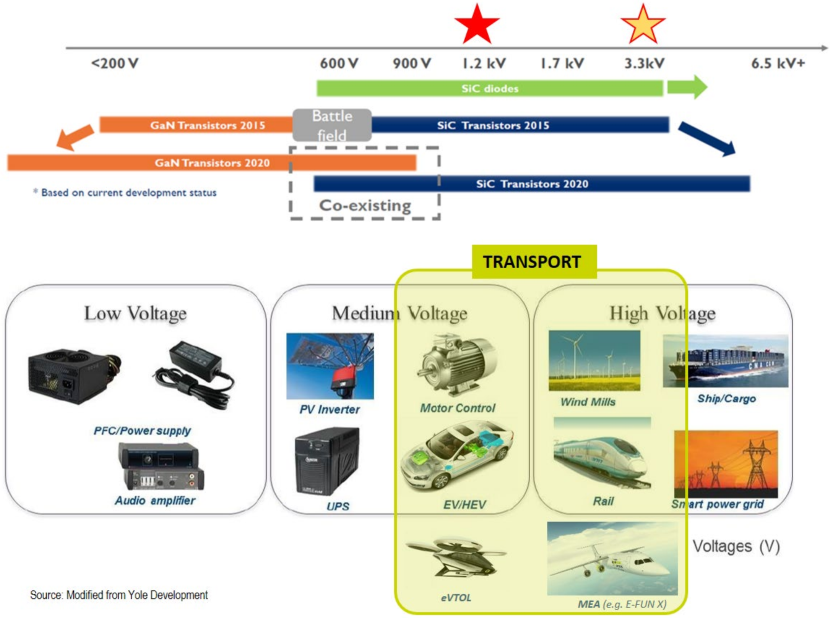
SiCRET

Silicon Carbide (MOSFET) Reliability Evaluation for Transport

End-user oriented project focused on

- **Test for SiC :** Definition of test procedures and methodologies adapted to user mission profiles (**dedicated SiC technology qualification**)
- **Design for SiC :** Establishment of mitigation solution (with respect to end-user MP) such as design recommendation (e.g.Derating rules for safety margins, etc.)

Context



Source: Modified from Yole Development

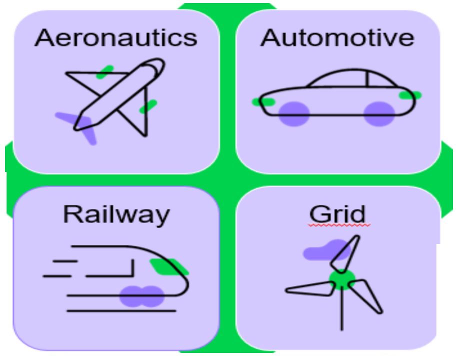
- **Future electrification technologies** require drastic improvements of power electronics. **SiC MOSFET are key enablers**
- **Reliability/ lifetime are mandatory for SiC adoption**
- Convergence of applications / high reliability requirements
- **Strong investment of industry is necessary to adapt qualification approach and design rules**

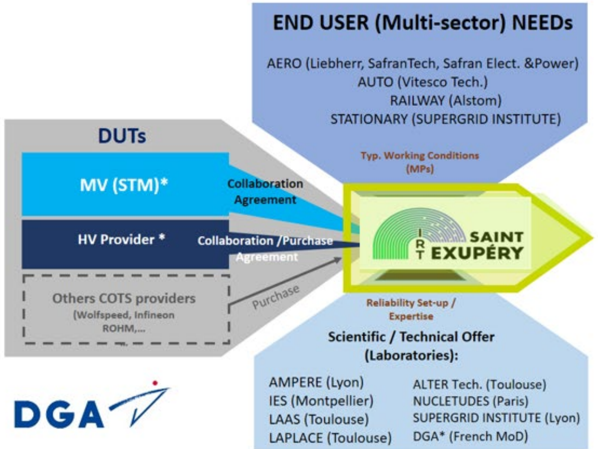
~5.3 M€ (50% Public* - 50% Private)

*ANR: French National Research Agency

36 months (May 2020 to Apr 2023)

Project members and partners





END USER (Multi-sector) NEEDs

AERO (Liebherr, SafranTech, Safran Elect. &Power)
AUTO (Vitesco Tech.)
RAILWAY (Alstom)
STATIONARY (SUPERGRID INSTITUTE)

Typ. Working Conditions (MPs)

DUTs

MV (STM)* — Collaboration Agreement

HV Provider * — Collaboration /Purchase Agreement

Others COTS providers (Wolfspeed, Infineon ROHM,... — Purchase

Reliability Set-up / Expertise

Scientific / Technical Offer (Laboratories):

AMPERE (Lyon)
IES (Montpellier)
LAAS (Toulouse)
LAPLACE (Toulouse)
ALTER Tech. (Toulouse)
NUCLETUDES (Paris)
SUPERGRID INSTITUTE (Lyon)
DGA* (French MoD)

SICRET Program: What's NEXT !

Discussion starting on 2022-Q2

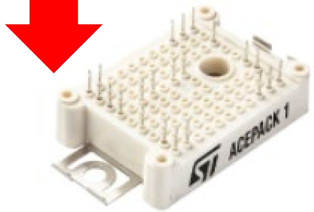
**Qualification Test plan Definition
(Proposal)**

Guidelines definition (SOA, Design rules, …)

At discrete component level

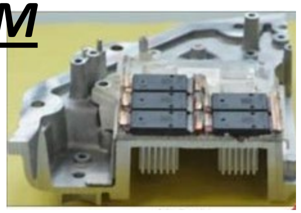
SiCRET
Silicon Carbide Reliability Evaluation for Transport

At Power Module level including other studies/tests.



- Low pressure, humidity,
- Thermal management (power cycling, temperature cycling)
- EMC emission/immunity

➡ ***Enhanced by the collaboration with STM (associate Partner of the project)***



Source: ST Microelectronics

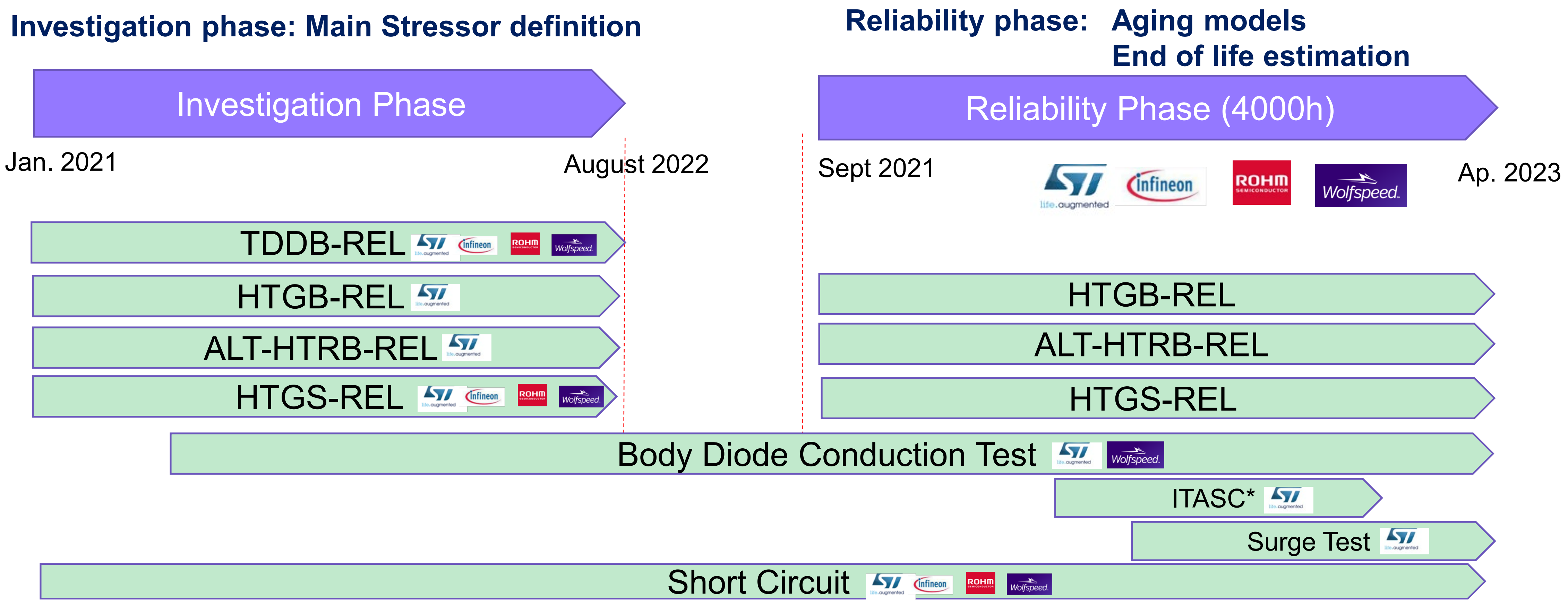
SiCRET+

NEXT WS on 16.11.2022

Silicon Carbide Reliability Evaluation for Transport

Medium Voltage Reliability Test Plan

Optimization Methodological Approach (costs-effectiveness)



Investigation phase: Main Stressor definition

Reliability phase: Aging models
End of life estimation

Investigation Phase

Jan. 2021

August 2022

Reliability Phase (4000h)

Sept 2021

ST life.augmented, infineon, ROHM SEMICONDUCTOR, Wolfspeed

Ap. 2023

TDDB-REL ST infineon ROHM Wolfspeed

HTGB-REL ST

ALT-HTRB-REL ST

HTGS-REL ST infineon ROHM Wolfspeed

HTGB-REL

ALT-HTRB-REL

HTGS-REL

Body Diode Conduction Test ST Wolfspeed

ITASC* ST

Surge Test ST

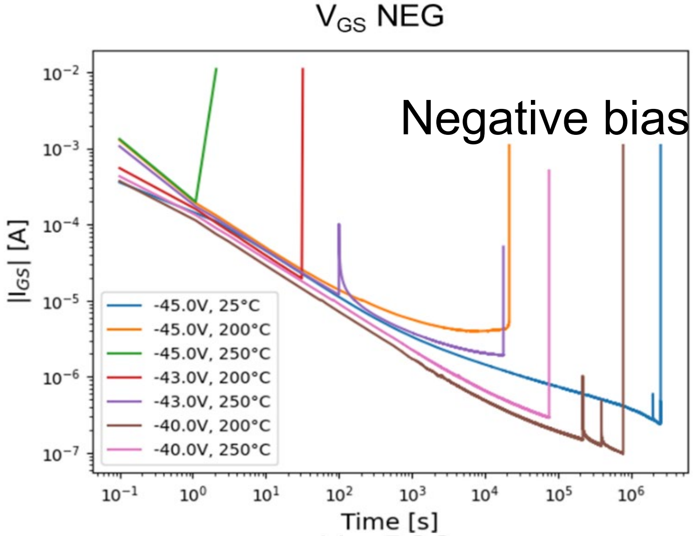
Short Circuit ST infineon ROHM Wolfspeed

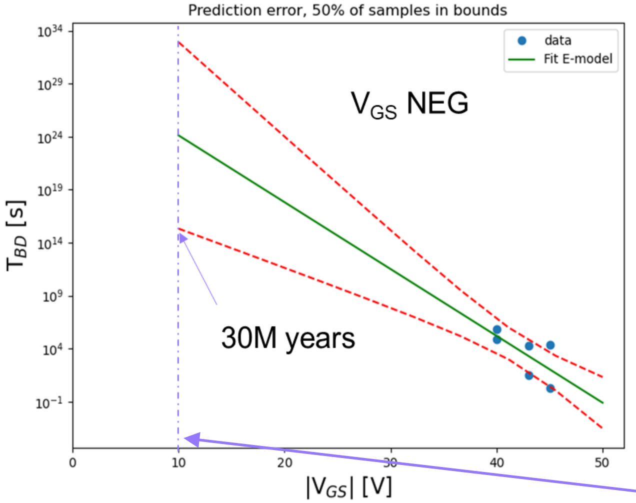
*Inverter Test with Accelerate Switching Condition

« REL » → above usual qualification time, up to EoL or degradation to derive ageing law

Investigation Test Plan: TDDB-REL Results

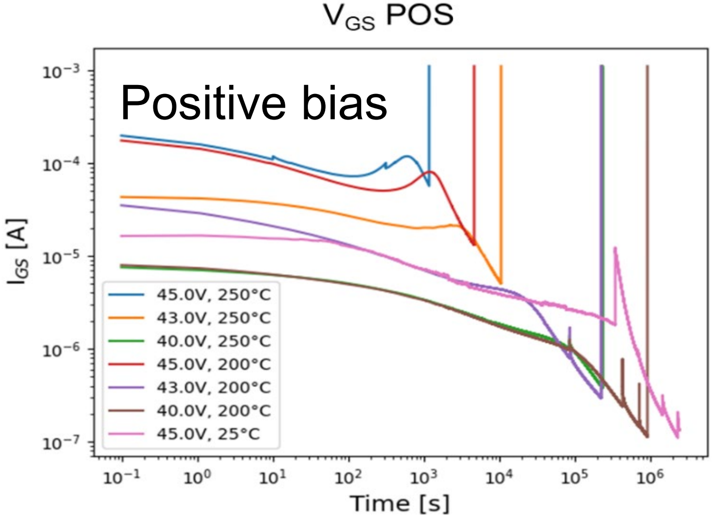
Investigation on TDDB for gate oxide lifetime prediction (STM-G2)

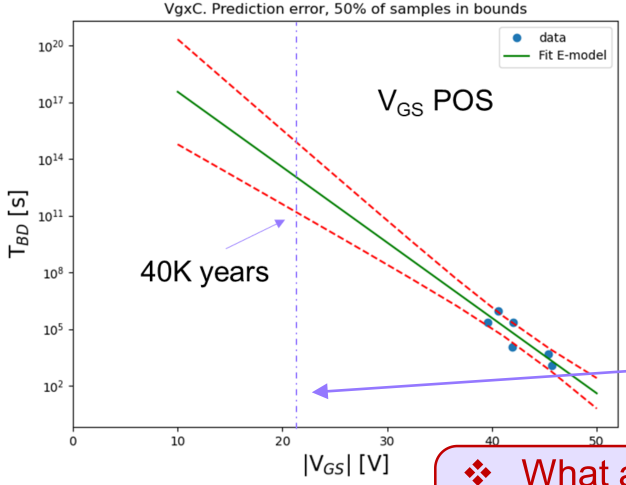




Lifetime projection obtained with E-model (most pessimistic model)
+ Prediction Error (50%) in Red dotted lines (because we are using very few components per test condition).

Max Negative V_{GS} rating (-10V)





Max Positive V_{GS} rating (22V)

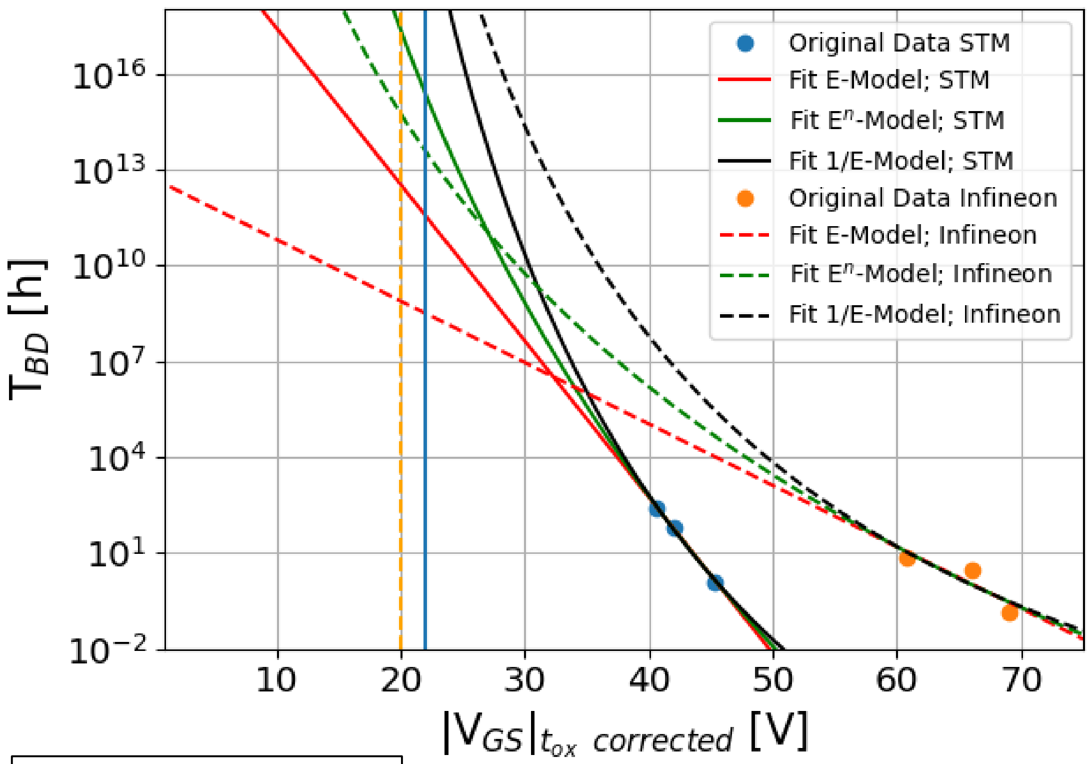
- ✓ Very high life expectancy (> 40K years) @ Absolute Max V_{GS} rating (-10V/22V) → Robust Gate oxide
- ✓ Negative bias were performed **for the first time**

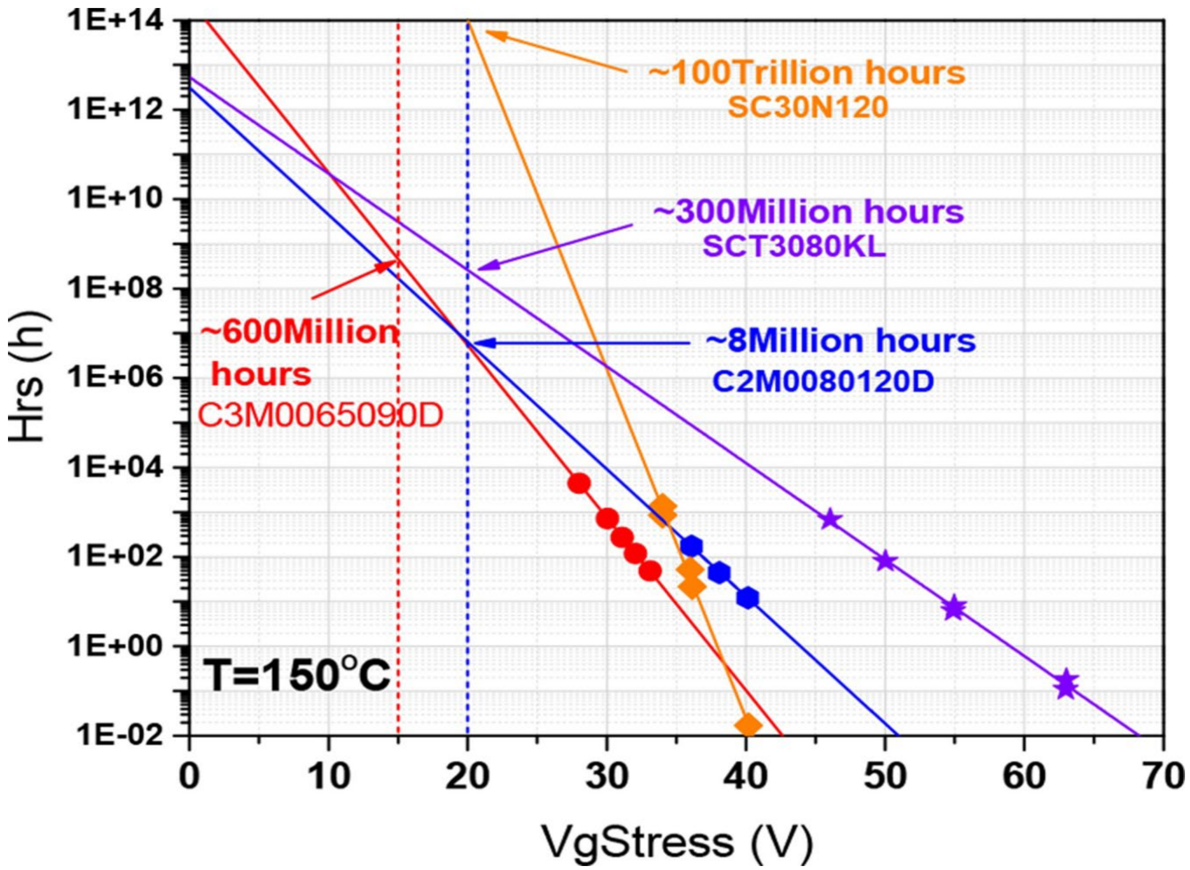
- ❖ What about prediction accuracy and consistency (Vgs too large with respect to FN threshold)?
- ❖ Only 1 sample per condition - No statistic yet
- ❖ Some phenomena yet to be studied (e.g. Bump on positive bias)

Lifetime projections of gate oxide comparison

STM vs Infineon Trench and vs state of the art

- Comparison between STM and Infineon; VGS POS





Max rating temperature :
- STM : 200 °C
- Infineon : 175 °C

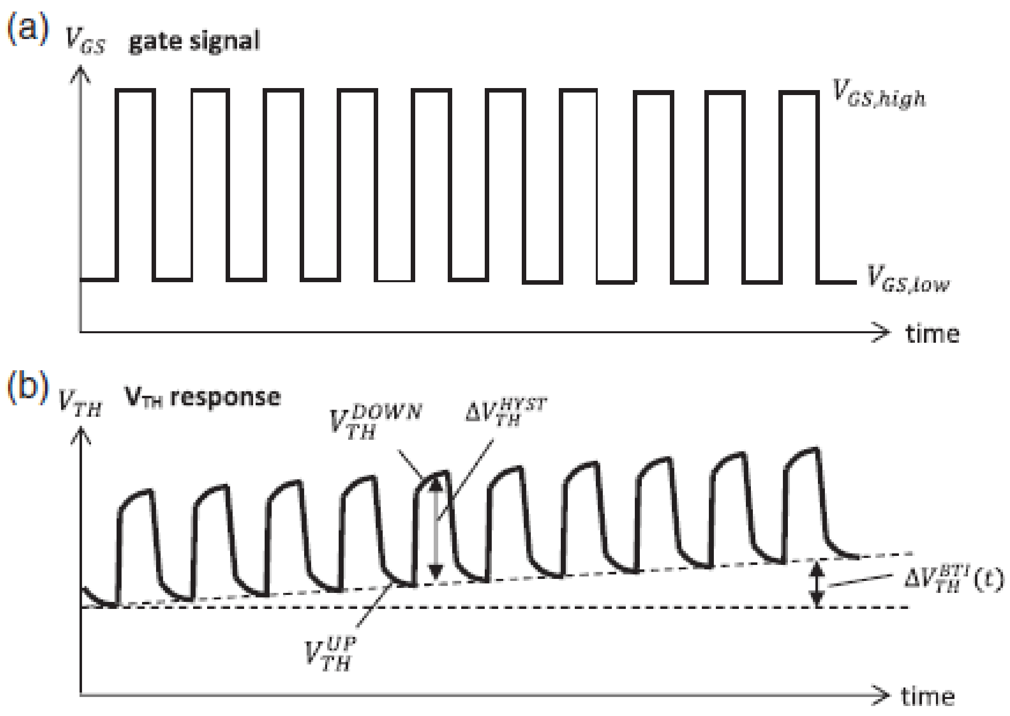
- Slope T_{BD} STM > Slope T_{BD} Infineon

✓ Very high life expectancy @ Absolute Max VGS rating
✓ Results consistent with other publications

Jun Wang and Xi Jiang,"Review and analysis of SiC MOSFETs' ruggedness and reliability" IET Power Electron., 2020, Vol. 13 Iss. 3, pp. 445-455

Need of reliability insight

at semiconductor (die) level



T. Aichinger, et al., Microelectronics Reliability 80 (2018) 68-78.

How to discriminate between reversible (recovery) and not reversible phenomena (aging) !!

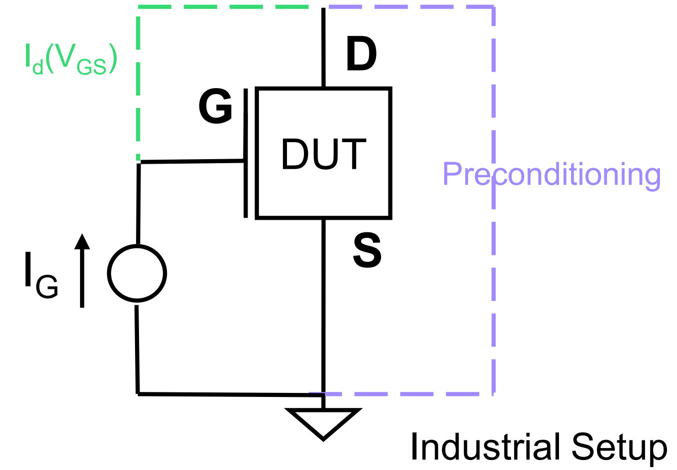
Vth Characterization

VTH protocol definition

V_{th} measurement @ Id = 1 mA

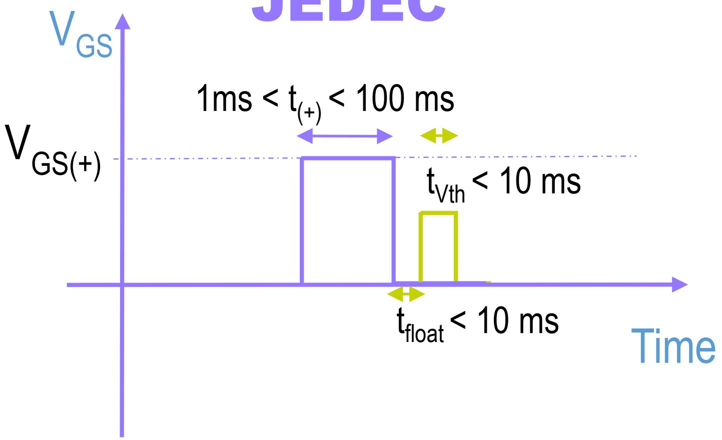
Unipolar

Bipolar

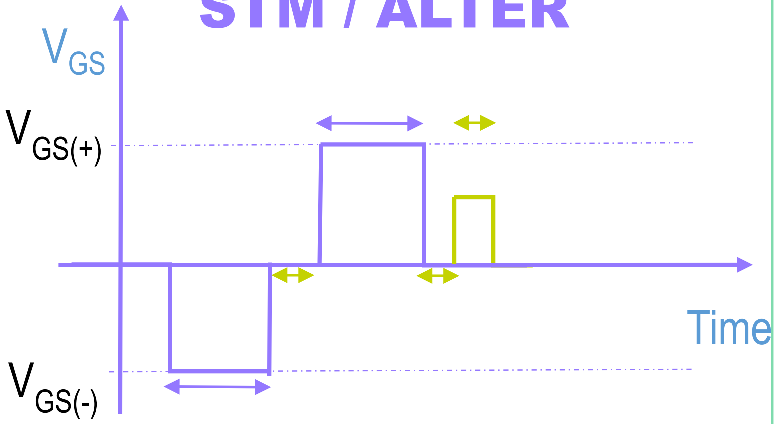


Industrial Setup

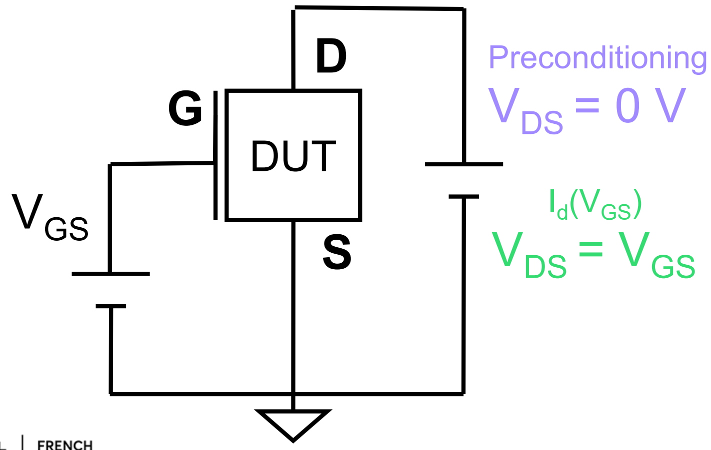
JEDEC



STM / ALTER

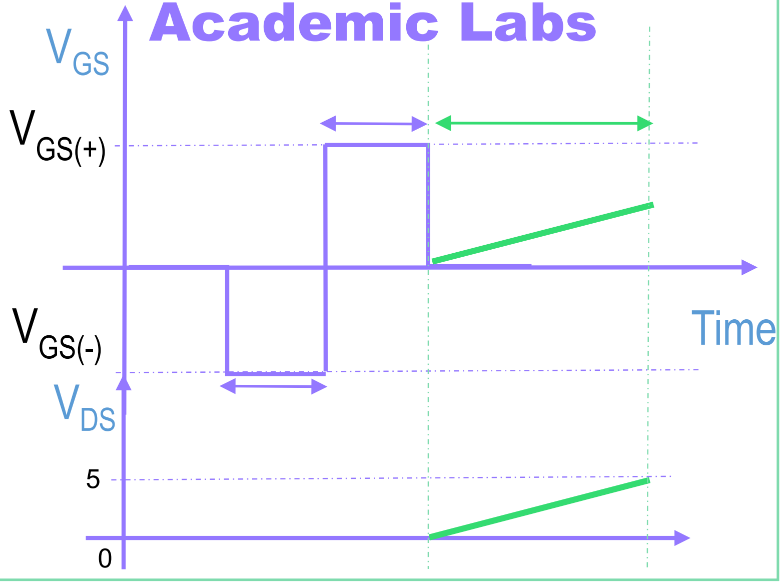


SiCRET setup

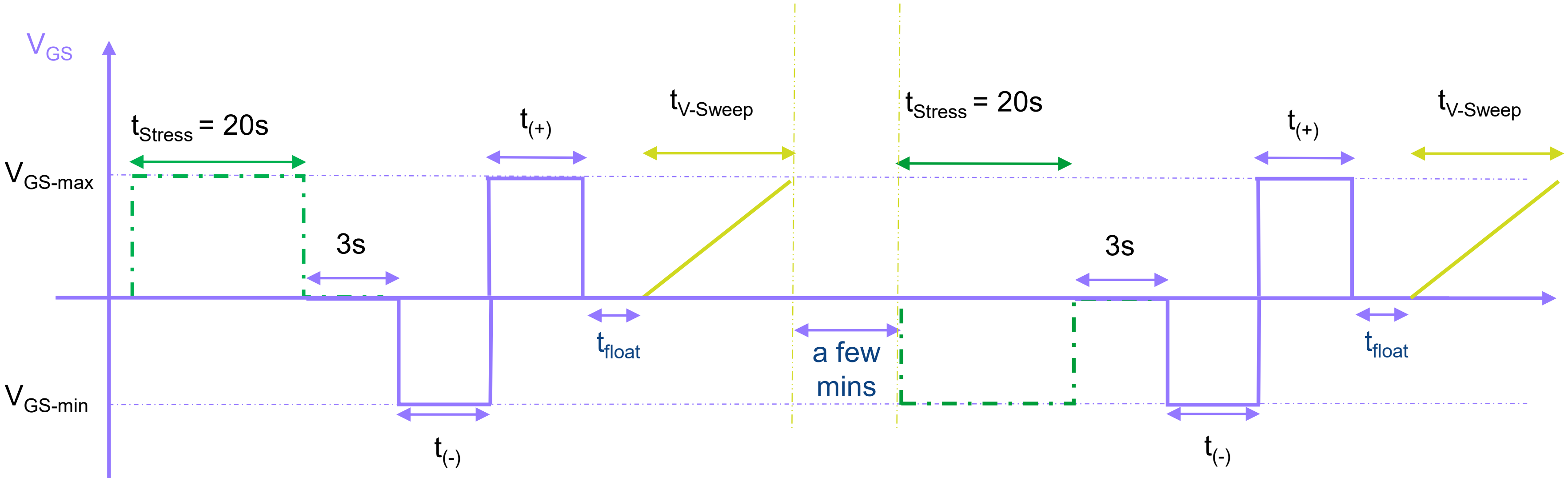


Related to B1505A

Academic Labs

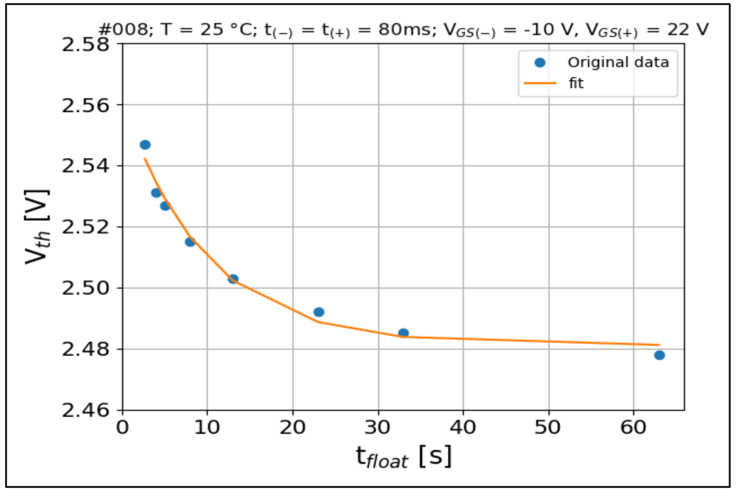


Influence of pre-conditioning on Vth measurement and time for read-out



➢ Influence of t_{float}

t_{float} delay impact on the Vth value



➢ Influence of positive / negative stress

Pre-conditioning robustness against device “normal operation history”

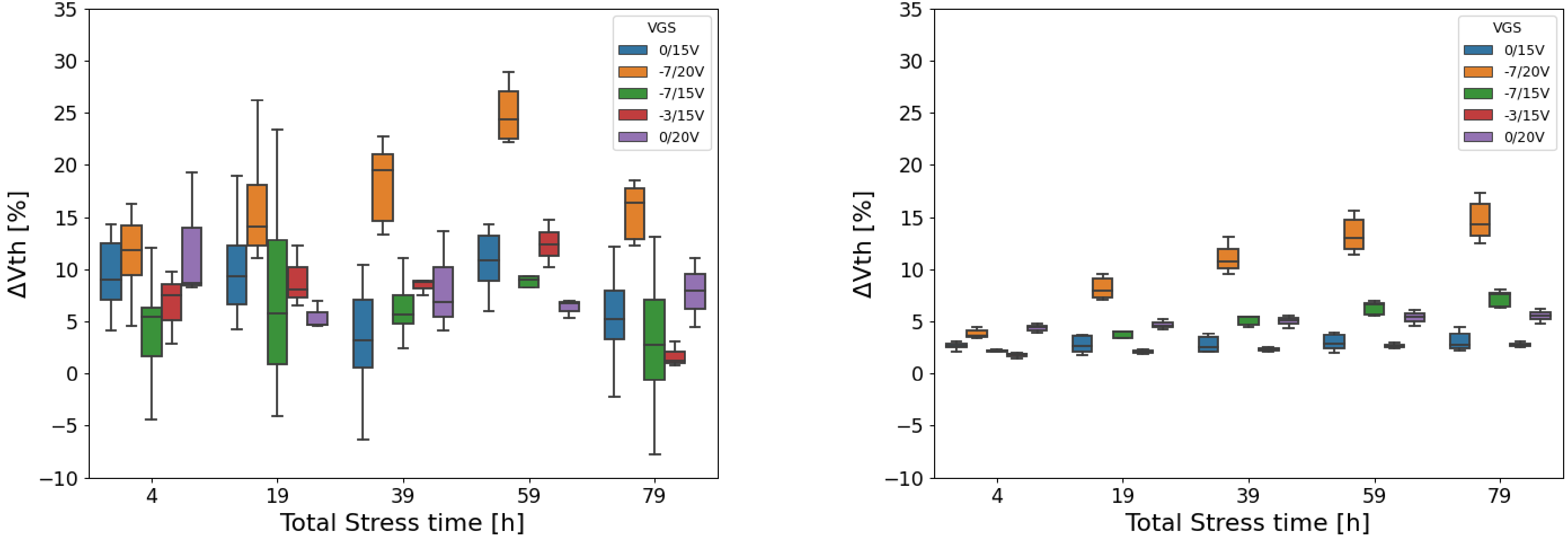
Pre-conditionning Method with tfloat=0	$\Delta V_{th\text{-}pos}$ Positive Stress of 20s	$\Delta V_{th\text{-}neg}$ Negative Stress of 20s	V_{th} (V)
Positive only	77 mv	144 mV	3.19
Negative + Positive	1 mV	14 mV	3.15

Vth Characterization

Example of stable Vth measurement

Without preconditioning

With SiCRET/JEP184 preconditioning



- ❖ Random behaviors in the case of Vth measurements without preconditioning

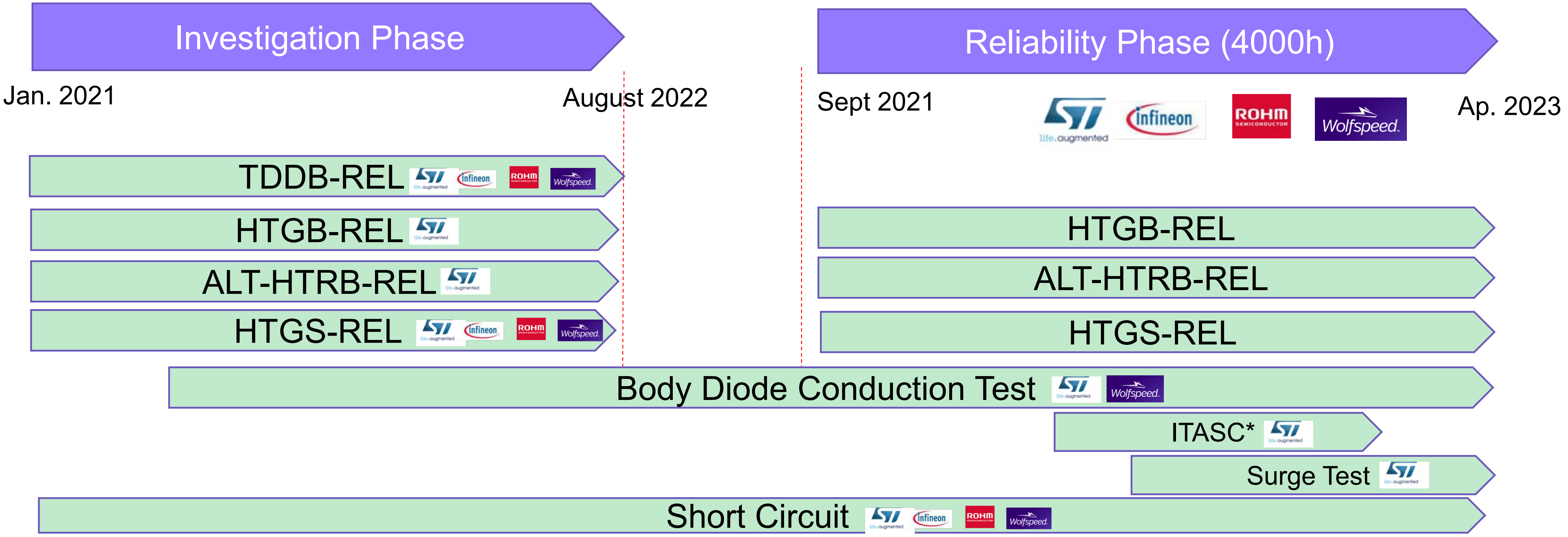
- ✓ Very stable and robust measurement of Vth (main aging indicator)
- ✓ True monitoring of Vth degradation
- ✓ SiCRET Vth method deployable on ALL environment (Research / Industry)

Medium Voltage Reliability Test Plan

Optimization Methodological Approach (costs-effectiveness)

Investigation phase: Main Stressor definition

Reliability phase: Aging models
End of life estimation



Investigation Phase

Jan. 2021

August 2022

Reliability Phase (4000h)

Sept 2021

Ap. 2023

TDDB-REL

HTGB-REL

ALT-HTRB-REL

HTGS-REL

HTGB-REL

ALT-HTRB-REL

HTGS-REL

Body Diode Conduction Test

ITASC*

Surge Test

Short Circuit

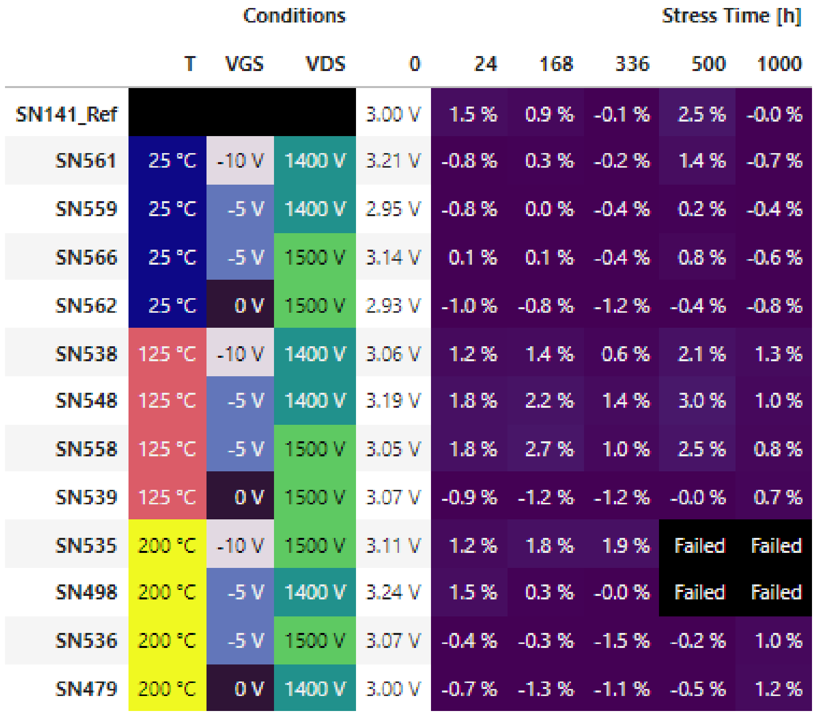
*Inverter Test with Accelerate Switching Condition

« REL » → above usual qualification time, up to EoL or degradation to derive ageing law

HTRB : Vth (1mA) drift results - ST Gen 2

Comparison between Investigation / Reliability

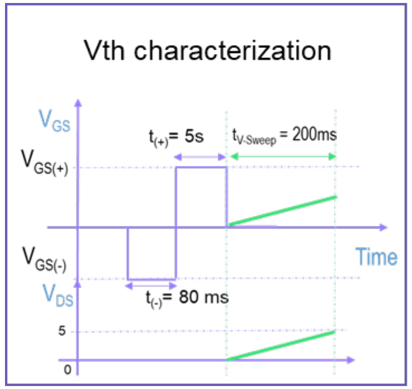
Investigation phase Results



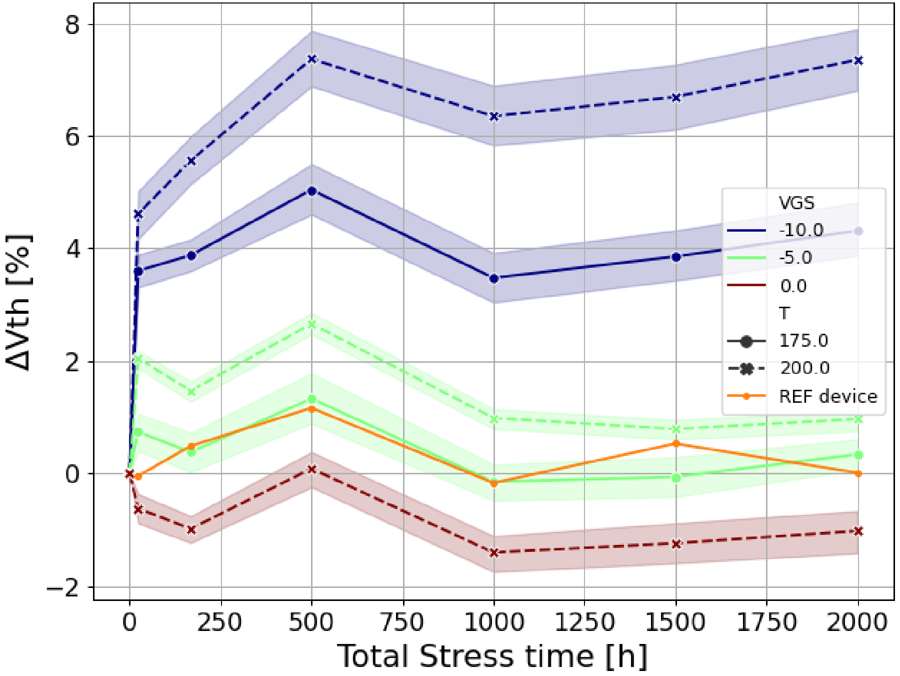
	Conditions			Stress Time [h]					
	T	VGS	VDS	0	24	168	336	500	1000
SN141_Ref				3.00 V	1.5 %	0.9 %	-0.1 %	2.5 %	-0.0 %
SN561	25 °C	-10 V	1400 V	3.21 V	-0.8 %	0.3 %	-0.2 %	1.4 %	-0.7 %
SN559	25 °C	-5 V	1400 V	2.95 V	-0.8 %	0.0 %	-0.4 %	0.2 %	-0.4 %
SN566	25 °C	-5 V	1500 V	3.14 V	0.1 %	0.1 %	-0.4 %	0.8 %	-0.6 %
SN562	25 °C	0 V	1500 V	2.93 V	-1.0 %	-0.8 %	-1.2 %	-0.4 %	-0.8 %
SN538	125 °C	-10 V	1400 V	3.06 V	1.2 %	1.4 %	0.6 %	2.1 %	1.3 %
SN548	125 °C	-5 V	1400 V	3.19 V	1.8 %	2.2 %	1.4 %	3.0 %	1.0 %
SN558	125 °C	-5 V	1500 V	3.05 V	1.8 %	2.7 %	1.0 %	2.5 %	0.8 %
SN539	125 °C	0 V	1500 V	3.07 V	-0.9 %	-1.2 %	-1.2 %	-0.0 %	0.7 %
SN535	200 °C	-10 V	1500 V	3.11 V	1.2 %	1.8 %	1.9 %	Failed	Failed
SN498	200 °C	-5 V	1400 V	3.24 V	1.5 %	0.3 %	-0.0 %	Failed	Failed
SN536	200 °C	-5 V	1500 V	3.07 V	-0.4 %	-0.3 %	-1.5 %	-0.2 %	1.0 %
SN479	200 °C	0 V	1400 V	3.00 V	-0.7 %	-1.3 %	-1.1 %	-0.5 %	1.2 %

- ✓ No significant drift on any parameter

- ❖ 2 failures analyzed.
- ❖ No conclusion on these failures



Reliability phase Results @Vds = 1200V



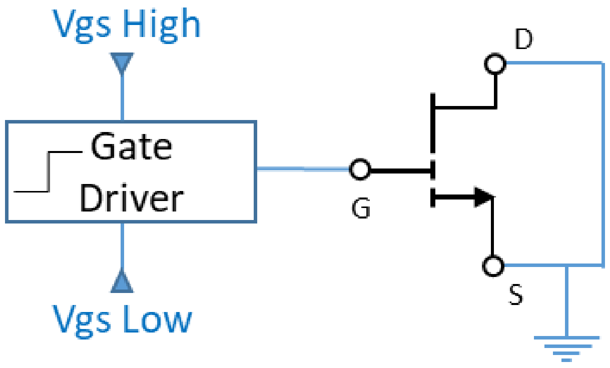
- ✓ Vth drift < 8%
- ✓ Vth variation is mainly due to negative Vgs
- ✓ Very Robust to HTRB

- ❖ No Ageing law regarding static Vds voltage

HTGS investigation phase One Week

Same DoE for each Manufacturer (excepted Vgs values adapted per datasheet)

Glossary (from datasheet):
- Vgs,on: Recommended turn-on gate voltage
- Vgs,off: Recommended turn-off gate voltage
- VgMax: Max positive transient voltage
- VgMin: Min negative transient voltage
- VgsAv: Average value between VgsMin and Vgs,OFF



HTGS DoE	Gate voltage	Temperature	Frequency	Duty cycle	Qty
Condition 1	Vgs,off / Vgs,on	25°C	500 kHz	20%	3
Condition 2	VgsMin /Vgs,on	25°C	500 kHz	20%	3
Condition 3	VgsMin / VgsMax	25°C	500 kHz	20%	3
Condition 4	Vgs,off / Vgs,on	25°C	500 kHz	80% (*)	3
Condition 5	VgsMin / Vgs,on	25°C	500 kHz	80% (*)	3
Condition 6	Vgs,off / Vgs,on	125°C	500 kHz	20%	3
Condition 7	VgsMin / VgsMax	125°C	500 kHz	20%	3
Condition 8	Vgs,off / Vgs,on	175°C	500 kHz	20%	3
Condition 9	VgsMin / Vgs,on	175°C	500 kHz	20%	3
Condition 10	VgsMin / VgsMax	175°C	500 kHz	20%	3
Condition 11	Vgs,off / VgsMax	175°C	500 kHz	20%	3
Condition 12	VgsAv / Vgs,on	175°C	500 kHz	20%	3

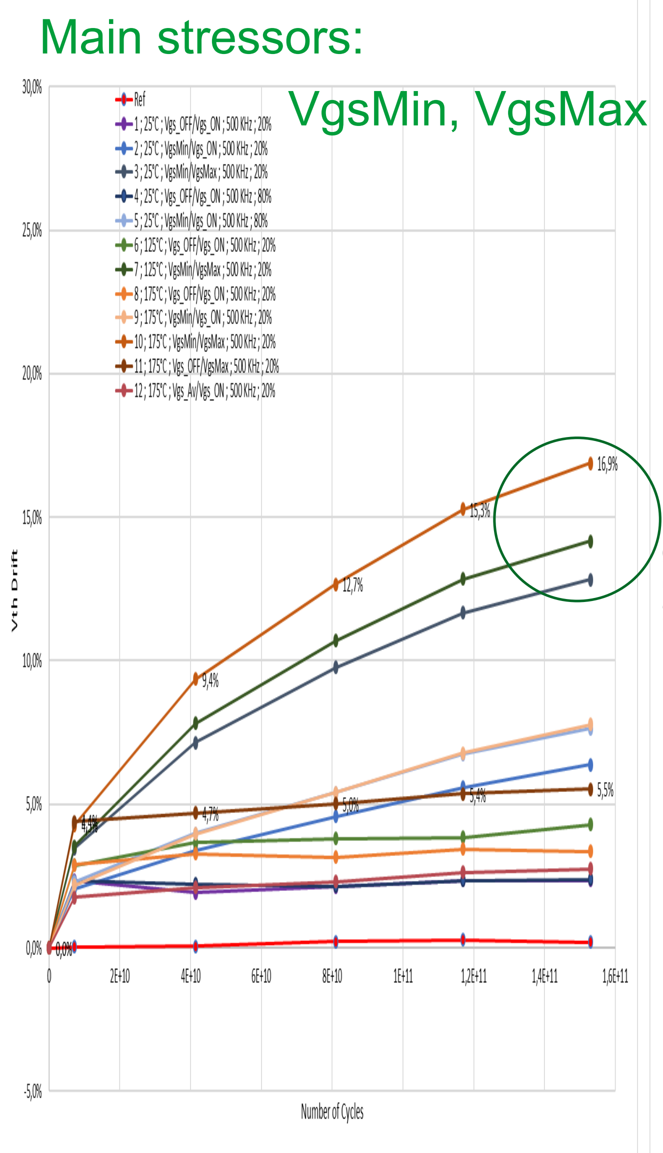
Note (*): DC = 80% means 80% ON, 20% OFF

HTGS investigation phase One Week

Vth (1mA) drift evolution

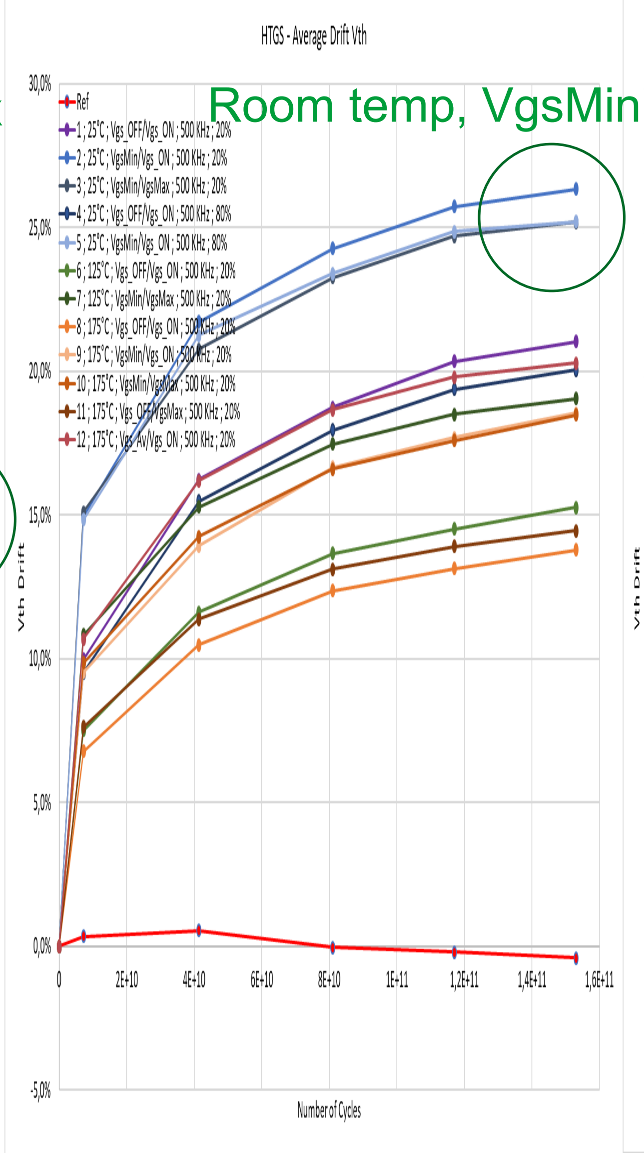
DUT A – Trench

Main stressors:



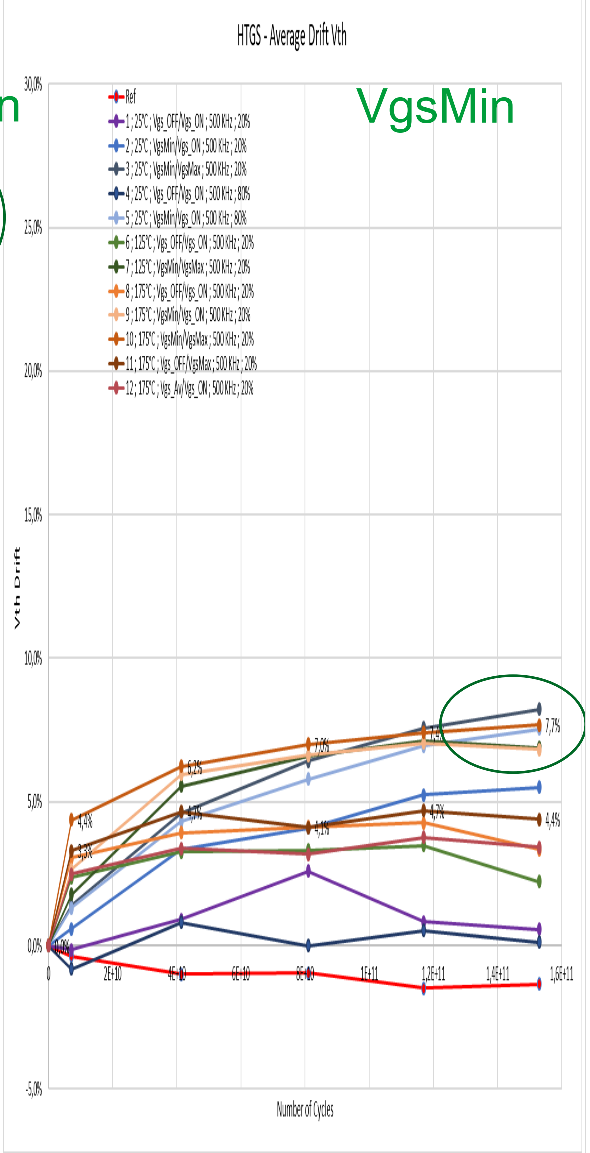
VgsMin, VgsMax

DUT B - Planar



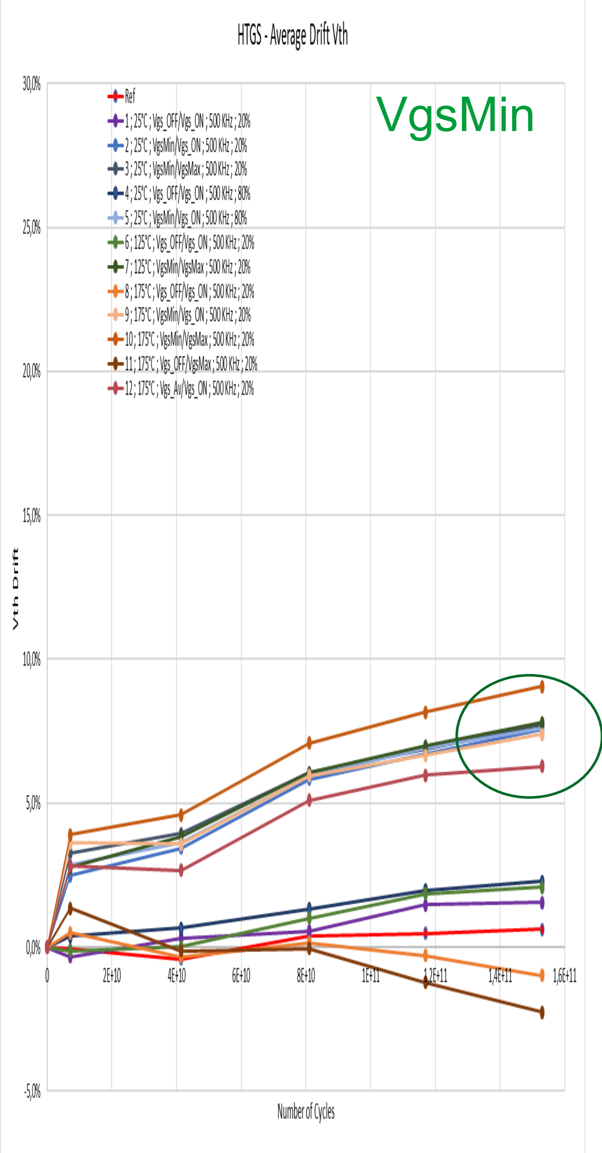
Room temp, VgsMin

DUT C - Trench



VgsMin

DUT D



VgsMin

STM Gen 2 – Investigation and Reliability Conclusions

Presently Under discussion at JEDEC

HTRB

No significant drift with Drain Voltage

Vth variation is due to VGS (-10V)

→ very robust to HTRB

→ next studies : DRB “Dynamic Reverse Bias”

HTGS

On ST Gen 2, main stressors causing V_{th} drift are :

- Temperature, VgsMin (and VgsMax?), commutation

Note: Number of cycles during application operating life is in the range between 10^{12} and 10^{13}

In order to know the main stressors governing the other DUTs HTGS
We decided to investigate a one week HTGS:

- Maximum available test bench frequency (500 KHz)
- Maximum and recommended Vgs values per datasheet
- Temperature influence (up to maximum rating value)

HTGB

The main stressors causing V_{th} and R_{DSon} drifts are related to :

- Temperature (200 °C).
- Gate voltages (specially if out of spec).
- Vth drift less than 10% after 10 years with an Automotive MP (Inverter)

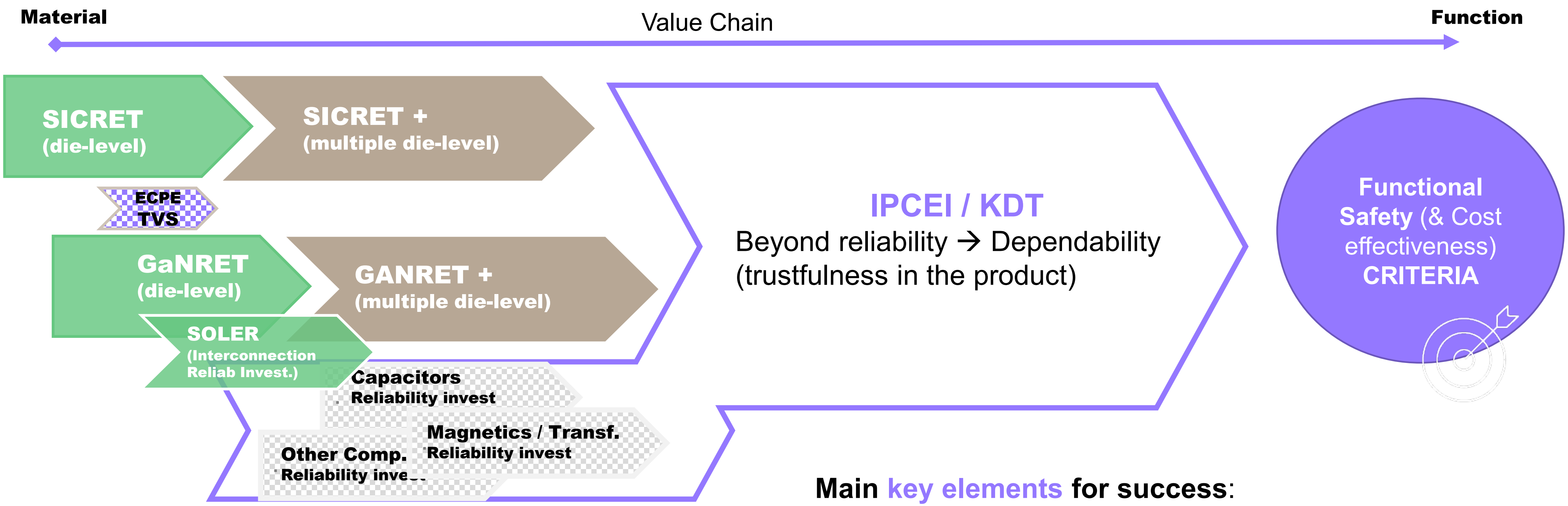
- ΔVth_{HTGB} (static stress) < ΔVth_{HTGS} (dynamic stress)

→ Dynamic stress is worse than the static one

Next step : find aging laws for HTGS

Synergy between collaborative Project

Toward dependable - "Trustfull" - WBG based power electronics



Material

Value Chain

Function

SICRET
(die-level)

SICRET +
(multiple die-level)

ECPE
TVS

GaNRET
(die-level)

GANRET +
(multiple die-level)

SOLER
(Interconnection Reliab Invest.)

Capacitors
Reliability invest

Magnetics / Transf.
Reliability invest

Other Comp.
Reliability inve

IPCEI / KDT
Beyond reliability → Dependability
(trustfulness in the product)

Functional Safety (& Cost effectiveness)
CRITERIA

🟩 Started (National Funding PIA / France 2030)
▨ Started (EU Funding - ECPE)
🟫 Planned but Not yet started / funded
░ Potential (yet to be discussed)

SICRET = SiC (MOSFET) Reliability Evaluation for Transport
GANRET = GaN (power) Reliability Evaluation for Transport

Main key elements for success:

- Converge on **common needs** across SC: converge on critical usage profile parameters (e.g. DT, dV/dt, …) - relevant for degradation)
- Leveraging on **existing knowledge** : Sharing information and best practice on test-for-reliability / design-for-reliability (see AEQ324)
- Tackling **functional safety** for given SC case study: identify and focusing efforts on critical path on end-to-end value chain (e.g. impact of cosmic radiation or short circuit event on function availability

Lighthouse activities

Connecting with Specialized Networking

In order to engage and establish a high level scientific and technical discussion with the most pertinent stakeholders , this task will be organized in three main types of activities:

- To organize focused workshops with industrial and/or scientific entities.
- Identify and stimulate the discussion and exchange with specialized professional networks such as the European Center for Power Electronics (ECPE) in Europe or the Center for Power Electronic Systems (CPES) in USA or their counterparts in other regions.

Centre Français Fiabilité

ECPE

CPES
Center for Power Electronics Systems

GIFAS

AnaDef

- Exchange and support international normalization bodies currently dealing with standardization of emerging WBG technologies, such as JEDEC, AEC, AFNOR, IEC…

JEDEC

AEC

afnor
NORMALISATION

IEC

AEG324

Conclusions and Perspectives

- ✓ PROOF is an important part of the Regional / National R&D asset and roadmap (toward electrification)
- ✓ IRT-SE consider PROOF as an essential partner to reach critical mass in WBG reliability projects

- ➢ Engage a discussion on evaluate how a more long term collaboration can be done (after PROOF PRRI)

- ✓ PROOF Scientific support (expertise and equipment) instrumental in running projects (e.g. SICRET, GANRET, …)

- ➢ Much more is ongoing and has to come yet:
  - Aging degradation monitoring by LFN (!?)
  - Dynamic behavior robustness (e.g. DRB, DBV, …) by ESD techniques (!?)
  - Interconnection degradation monitoring by RF detection (!?)
  - Device junction temperature for thermal monitoring and management (NRTW Rouen March 2023)
  - Use of NFS techniques to enhance EMC/I design (from device to board and back)
  - …

IRT SAINT EXUPÉRY

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anr agence nationale de la recherche