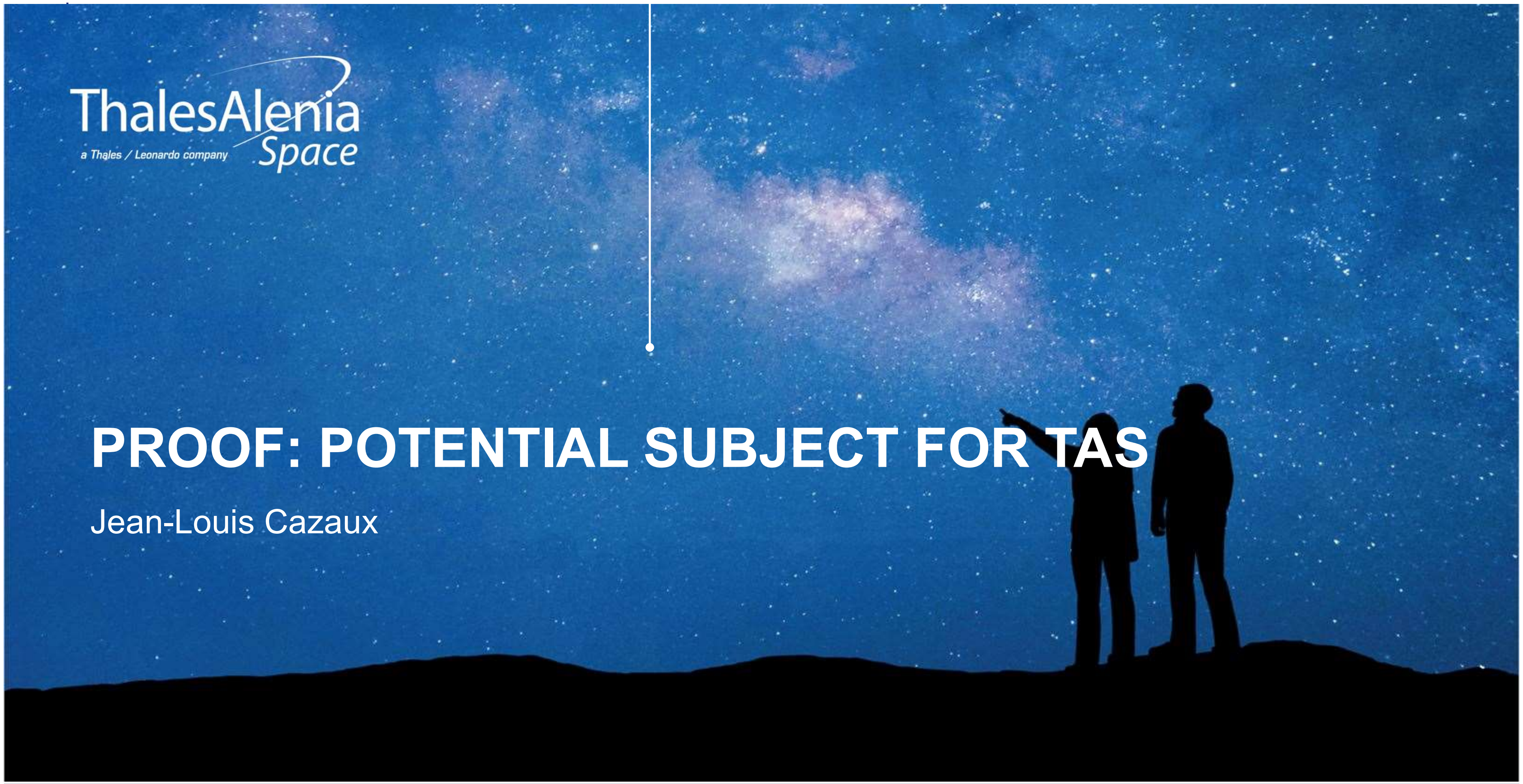

PROOF: POTENTIAL SUBJECT FOR TAS

Jean-Louis Cazaux

Date: 10/02/2021
Ref: Not referenced
Template: 83230347-DOC-TAS-EN-009

TAS MOTIVATION FOR PROOF

/// Thales Alenia Space is strongly supporting the PROOF Platform in LAAS

/// Large commonality of interests among the different stakeholders at local level: industry, LAAS, IRT StEx, CEA-Tech, CNES, …

/// GaN is a major priority in our EEE components roadmaps both for Microwave applications and DC/DC Supply applications.

/// TAS has already a large experience with these technologies and also a long history of collaboration with LAAS on this field.

POTENTIAL AREAS OF COLLABORATION

/// Ponctual short-term study about Noise performance assessment and modelling of mw GaN transistors

/// Characterization of very advanced GaN/Diamond mw Transistors. TAS to provide the transistors to LAAS as a validated contribution

/// Prepare and plan a possible PhD Thesis on mW GaN, on Noise or Reliability or both, to be proposed to CNES for co-funding in summer 2021, selection of a candidate early 2022 and start of PhD for September 2022. This could be re-inforced with an engineer internship in TAS in spring 2022 with the future PhD candidate.

/// Support of PROOF to TAS in the H2020 ELEGANT project (just kicked-off in Jan. 2021). It concerns GaN transistors and ICs from IMEC technology. This could be put in place in 2022.

/// Collaboration and/or support in NANO2022 IPCEI led by ST on Power GaN Technology. Transistors supposed to be available in 2022.

ANNEXES

INTRODUCTION

Plusieurs applications pour développer LNA GaN robustes :

- _ entre 22 GHz et 36 GHz.

Besoins :

- _ Validation modèle au niveau transistor en bruit et paramètres S dans des conditions de polarisations hors modèles (faibles Vds principalement, Vds=0V)
- _ Test des temps de recouvrement des transistors dans le cadre d'applications pulsées (état On /état Off), avec conditions d'overdrive état On/Off selon les profils de mission
- _ Test de tenue en robustesse des composants pour des conditions modèles poussées aux limites,
- _ introduction de switch de protection permettant de protéger LNA dans certains cas de figure (Mauvaise manipulation au sol, court-circuit antenne)

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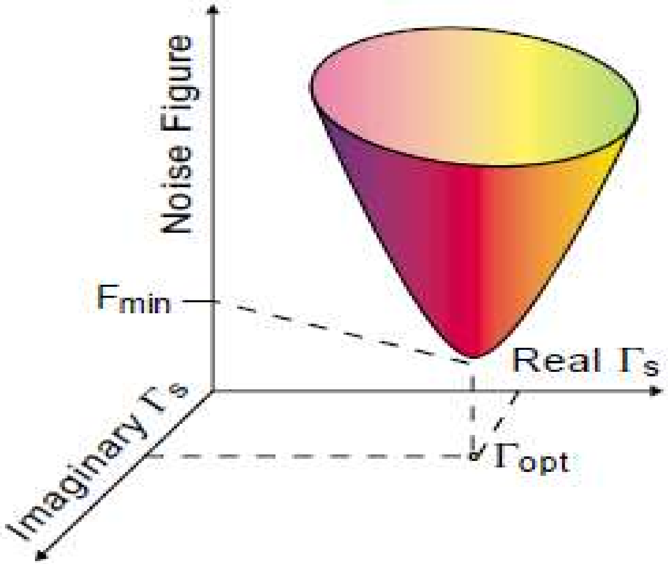
MESURES DES 4 PARAMÈTRES DE BRUIT

Figure 1: Noise Characterization

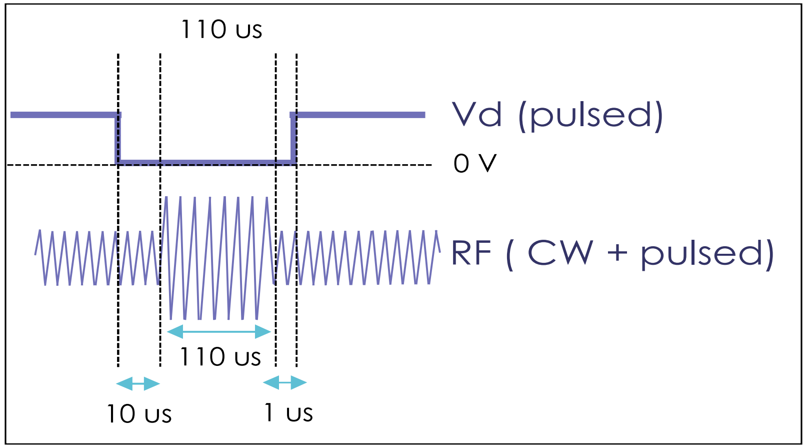


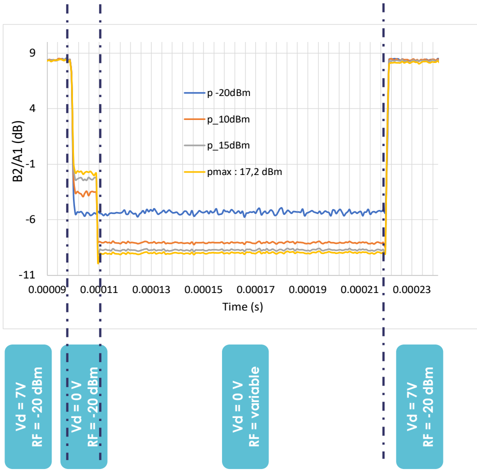
- Determines the Four Noise Parameters
  - Minimum Noise Figure
  - Real Part (Magnitude of Optimum Z, Y, or Γ
  - Imaginary Part (Angle) of Optimum Z, Y, or Γ
  - Equivalent Noise Resistance

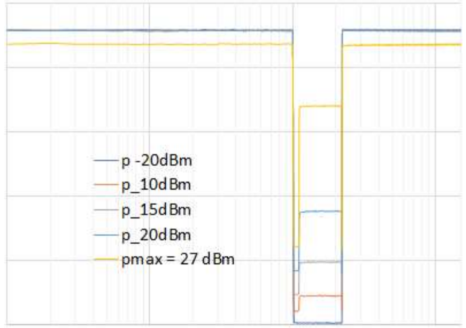
$$F = F_{min} + R_n/G_s \,|\, Y_s - Y_{opt} \,|$$

$$F = F_{min} + 4 r_n \frac{|\,\Gamma_s - \Gamma_{opt}\,|^2}{|\,1 + \Gamma_{opt}\,|^2 \,(1 - |\,\Gamma_s\,|^2)}$$

RECOVERY TIME PRINCIPLE







Valeur moyenne sur 10 impulsions

Signal RF constitué d'un train d'impulsions de 120 µs, avec différents rapports cyclique. 1.5 ms de période.
Durée d'exposition: variable.
Test réalisé à plusieurs niveaux de puissance : -20dBm, 10dBm, 15dBm, 20 dBm (si possible) et Pmax(dBm)

Influence de la fréquence de travail sur les effets de piège, des conditions d'adaptation ou de polarisation.

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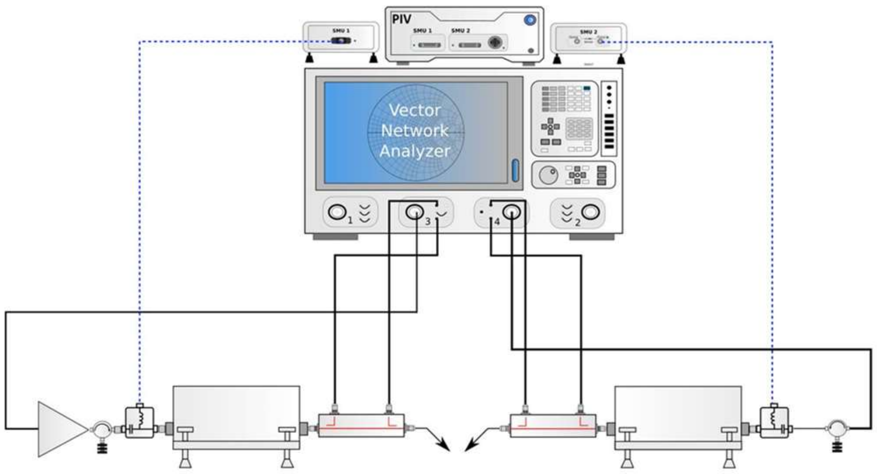
BANC DE MESURE EN AGRESSION



- Step 1 : Power Sweep until 3 dB compression
- Step 2 : S-parameters measurement @ - 10 dBm
- Step 3 : LP measurement @ 0 dBm
- Step 4 : S-parameters measurement @ -10 dBm
- Step 5 : LP measurement @ 3 dBm
- Step 6 : S-parameters measurement @ -10 dBm
- Step 7 : LP measurement @ 6 dBm
- Step 8 : S-parameters measurement @ -10 dBm
- Step 9 : LP measurement @ 9 dBm
- Step 10 : S-parameters measurement @ -10 dBm
- Step 11 : LP measurement @ 12 dBm
- Step 12 : S-parameters measurement @ -10 dBm
- Step 13 : LP measurement @ 15 dBm
- Step 14 : S-parameters measurement @ -10 dBm
- Step 15 : LP measurement @ 18 dBm
- Step 16 : S-parameters measurement @ -10 dBm
- Step 17 : LP measurement @ 21 dBm
- Step 18 : S-parameters measurement @ -10 dBm
- Step 19 : LP measurement @ 24 dBm
- Step 20 : S-parameters measurement @ -10 dBm

Synthétiseurs d'impédances 8-40 GHz =>conditions d'adaptations 50 Ω en sortie, agression CW ou pulsée, durée 1 min, pas de 3dB. Tuner revient sur 50 ohms après agression pour mesure linéaire, Mesure sur transistor ou sur circuit complet, état on ou état off

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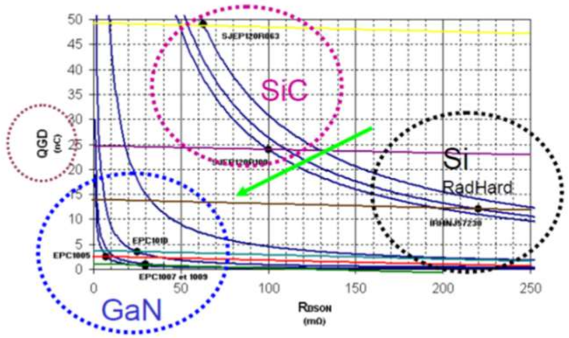
TAS-F GAN FOR SPACE POWER SUPPLIES

Use of a theorical Figure Of Merit on the application :



2011 : survey on wide band-gap transistors

- **Cost driven :**
  - « Wide-bandgap transistors seem less sensitive to radiations (TiD & SEE) »
  - -> no need of special die design to cope with space application
- **Criterias : replace Space qualified MOSFET**
  - Normally off switches
  - Bi-directional in current

GaN selected (vs SiC)

- **Tolerant to harsh environment (TID, SEE)**
- **Better integration**
- **Better Performance**

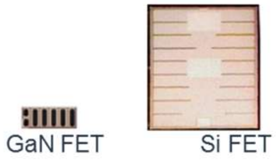
- **But :**
  - ***Maturity was to be improved***
  - ***Tricky Driving***
  - ***Packaging & Temperature***

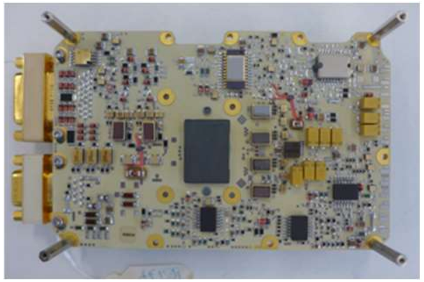
Characteristics		FET Technology			Comments
		Si	SiC	GaN	
Electrical	Ron	😐	☺	☺☺	
	Tsw	😐	☺	☺☺	
	Max Voltage	😐	☺☺	☺	
	Max Current	😐	☺☺	☺	
Environ.	Max Temp	😐	☺☺	☺	* : but high temp could be achieved (theorically)
	Thermal conduct.	😐	☺☺	☺	
	Radiation	😐			TBC
	Parameter stability	😐	☺	☺	TBC by tests
Manuf.	Wafer Size	😐	☹☹	😐	
	Process	😐	☹	?	For GaN : "seems" simple but few labs/manufacturers
	Die Size	😐	☺	☺☺	
Procur.	Availavility	😐	☹	☹	
	Cost	😐	?	?	SiC & GaN could be lower if radiation immuity and process
	Maturity	😐	☹	☹	but huge improvements on-going

TAS-F GAN FOR SPACE POWER SUPPLIES

TAS-F past experience :

- 2010 : Survey start-up
- 2012 : Evaluation in 10W for RF units
- 2014 : Selection & evaluation in 250W for RF units
- 2018 : Qualification & Production in 60W DCDC for digital unit



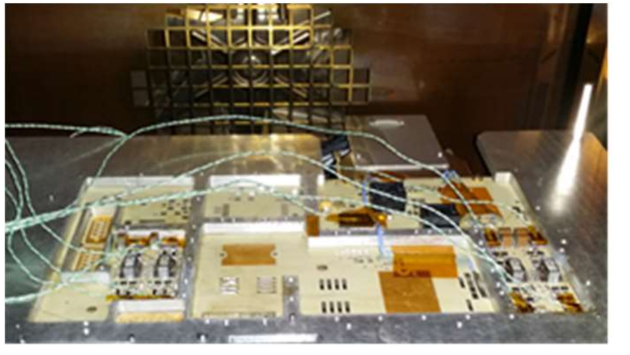


TAS-F GAN FOR SPACE POWER SUPPLIES

Additinol Tests

New/early technology

- to understand failure mechanisms
- to ensure robustness
- to define the safe operating area linked to the applications
- to reveal the technical limits



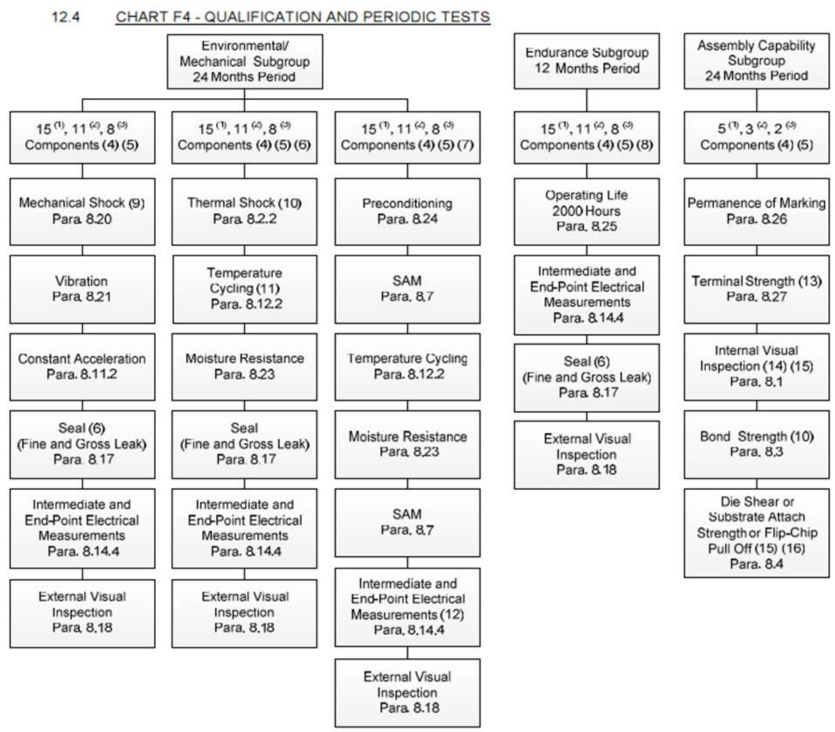
Additional evaluation done :

- Confirm the radiation robustness (heavy ion, TID, TNID,…)
- Electrical checks :
  - Gate-Source voltage limits
  - leakage currents drifts
  - on–resistance (Rdson) mastering
- Behavior at high temperature (190°C)

TAS-F GAN FOR SPACE POWER SUPPLIES

Qualification for HiRel Parts Under ESCC9000

- validated by French Space Agency (CNES)
- Several Endurance subgroups on subsequent lots
- Above ESCC9000 in life-test



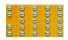
TAS-F GAN FOR SPACE POWER SUPPLIES

Feedback & way-forward

- MOSFET replacement (200V & below : most quantities and applications)
  - no EU/EC competitors : only asian/american manufacturers
  - Almost no sensitivity to radiation
  - Drivers and transistors shall be as close as possible
  - Space de-rating rules to be revisited :
    - Not consistent with manuf. recomm. : Vgs recomm. at ~80%.Vgsmax and de-rating at <75%.Vgsmax
    - Limit application : temperature below 110°C

  But limited SOA, linear mode "adventurous", no equivalent to PMOS
- More and more new needs on very high current (@ very low voltages)
  - Lowest Ron in switching application
  - Thermal draining & packaging

Transistors alone



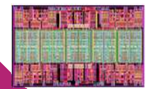
Transistors & drivers in same package

H2020 HeatPack

Transistors & drivers in same die

H2020 EleGaNT

GaNIC



ELEGANT

GaN Transistor Integrated Circuits

SPACE-10-TEC-2020 - Technologies for European non-dependence and competitiveness

01/01/2021 -> 31/12/2023 **Budget:**~2.5MEuro

Consortium: IMEC (B), TAS-B (B), TAS-F (F), Wurth (D), Mindcet (B), IEIC (F)

Objectives:

- p-GaN enhancement mode HEMTs and driver, GaN IC technology platform **for Point of Load converters**
- GaN power IC for low voltage (<50V) enabling very high current (>40A) switching frequencies in the range from 500kHz to
- Robustness against radiation TID up to 120krad and heavy ions 62.5 MeV (Xenon)
- Reduction of the inductive parasitics through monolithic integration of drivers and power devices (GaN-IC)
- Reduce the weight and size of the power converter passive inductor by 50% compared to state-of-the-art solution
- Demonstration of prototype **very high current space application**. Input voltage 5-12V, output voltage 0.5-1V, output current >40A, efficiency >90%
- Demonstration of prototype **low current space application**. Input voltage 5-12V, output voltage 0.5-1V, output current 10A, efficiency >90%
- Evaluation of the technology for **terrestrial applications**. Datacenter POL DCDC modules Input voltage 5-12V, output voltage 0.5-1V, output current >40A, efficiency >90%

Achievements up to date:

- Kick Off in January 2021

European Commission