



# Focus sur les activités fiabilité et Grand Gap

Présentation des projets en lien avec PROOF et perspectives pour une réflexion de structuration de l'écosystème électronique de puissance dans la région et en France

COS – PROOF  
04.02.2021 @ LAAS-CNRS

[Fabio.Coccetti@irt-saintexupery.com](mailto:Fabio.Coccetti@irt-saintexupery.com)

*Responsible of the “High Reliability” Center of Competence*



- Introduction: Context and Objective
- Overview of WBG activities for Power Electronics
- Focus SICRET:
  - From PoF to better test, better Design, (and better manufacturing)
  - Identification and deployment of the R&T program (beyond Q101, JEDEC)
  - Focus on collaboration with LAAS
- Conclusion and Perspectives

➤➤➤ Cofinancé par les membres industriels & l'État dans le cadre du PIA\* 

\*Le Programme d'investissements d'avenir



**Catalyse** → Accélération → Transfert

Bridging (COTS<sup>(1)</sup> based on) emerging technologies to harsh environment operation

**Reliability based on PoF analysis**  
(from component/cell to board/stack level)

- Comprehensive Risk (Lifetime & CFR) assessment methodology (FRAME)

**Natural Radiation immunity**

- Radiation induced failure mechanisms analysis and understanding

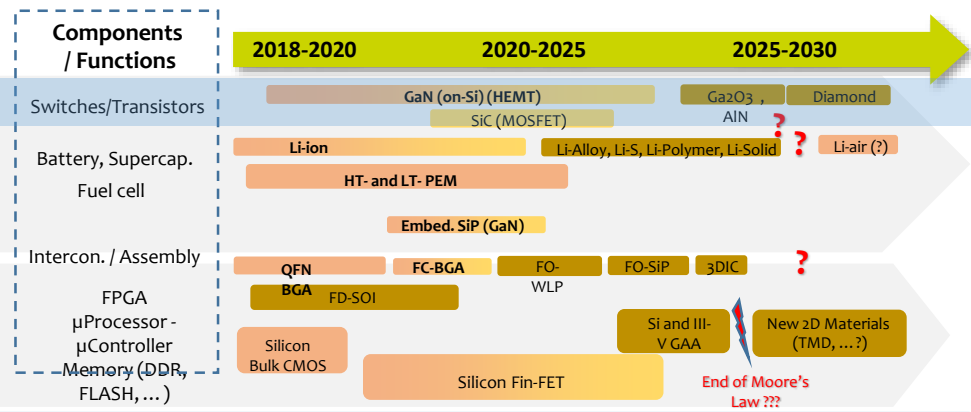
**Electromagnetic Compatibility (EMC) from NFS to System**

- Obsolescence management
- Fast Board prototyping and tool development for optimization / verification



(1) **Semiconductors** components (Deep Sub Micron (FDSOI, FinFET, 3D), WBG based transistor (GaN and SiC)...) and **Electrochemical** for energy sources/storage (Fuel cell, Li-X batteries, Supercapacitors); **Assembly and packaging solution** (High Power, High Density, High Frequency) SoC or SiP

# High Reliability Center of Competence: Roadmap



**Objectives**  
 Predictive / Diagnostic Reliability

**Reliability (CFR / EOL) / Obsolescence Management**

**Fast / Virtual Prototyping**  
 (DfR, EMC compliance, Technology Eval.)

**Certification Support**

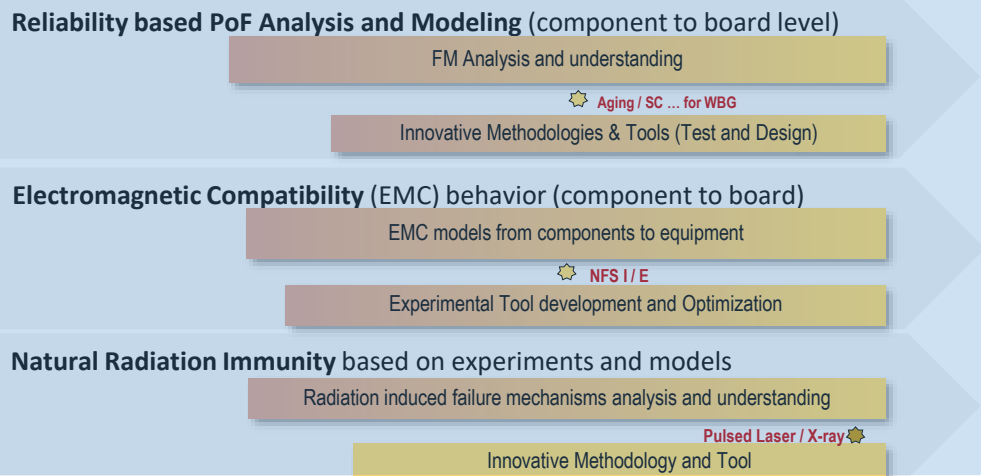
**WBG Activities**

**Component / Technology Roadmap**

More **Electrical Power** (propulsion / non propulsion)

More **DIGITAL** functions

**Implementation Roadmap**

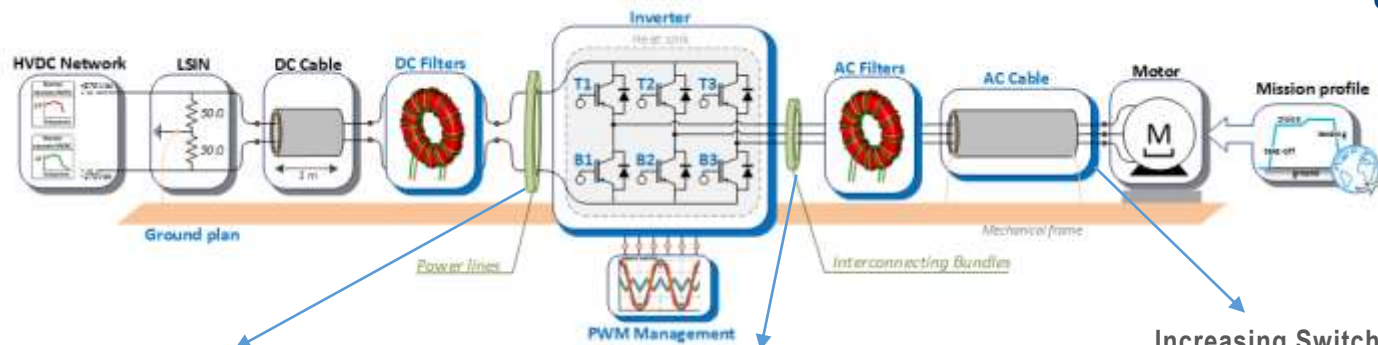


- Done
- Planned
- Opportunities

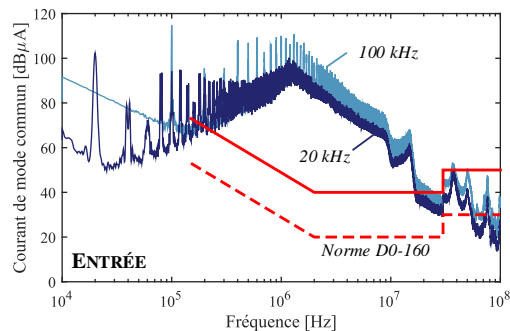
★ Platforms

? → Breakthrough needed to enable actual disruptive evolution (high risk / fundamental research)

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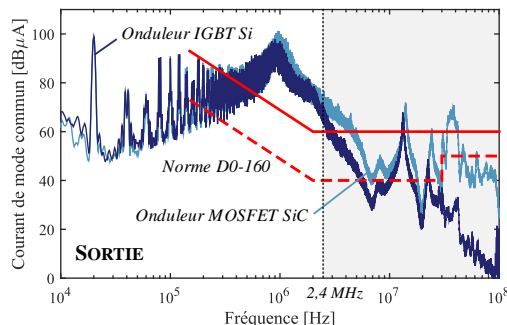


### Increasing Switching Frequency



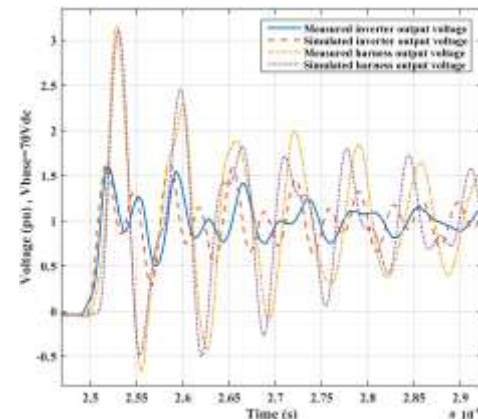
- » High CM Current
- » Heavy/bulky CM Filters

### Increasing Switching Speed



- » High CM Currents
- » Heavy/bulky CM Filters

### Increasing Switching Speed



- » High overvoltage on motors
- » Heavy/bulky DM Filters

# Project WBG: Overview

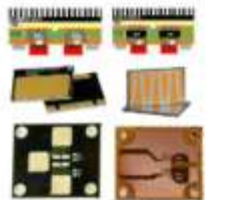


Multidisciplinary design optimization of electrical system

Control card & algorithm, optimized PWM, active gate driver



Cooling system optimization



GaN PCB embedded



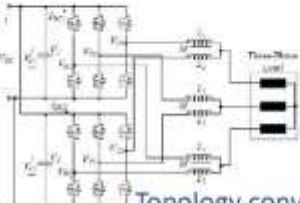
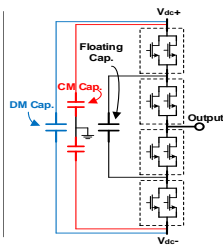
Innovative SiC power module

**High Efficiency & Integrated SiC & GaN Power Converters\***

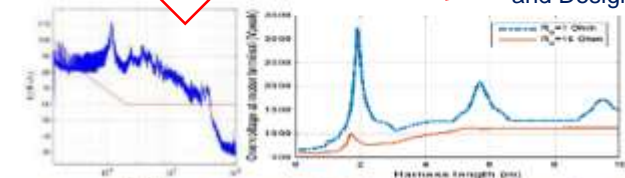


Component, power module & magnetics loss characterization

RF Modeling and Design



Topology converter



EMI, overvoltage & partial discharge impact evaluation .

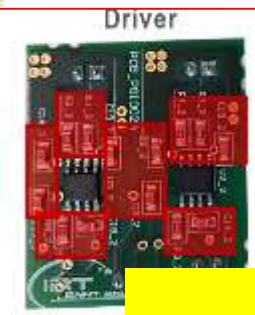
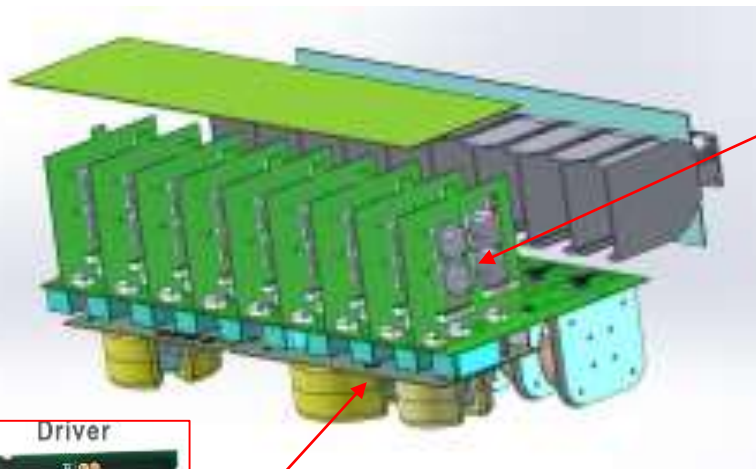


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# Integration in Complex Systems

Multiple-Stage Flying-Cap Three phases 70KW 540V  
 GaN (144 series & parallel)

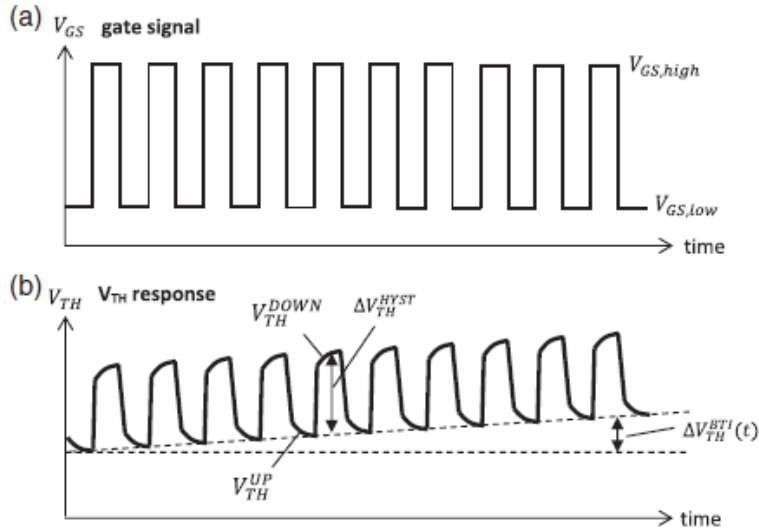


- How to take into account the drift of key parameter e.g.  $V_{th}$
- How to discriminate between die and higher complex integration level failures

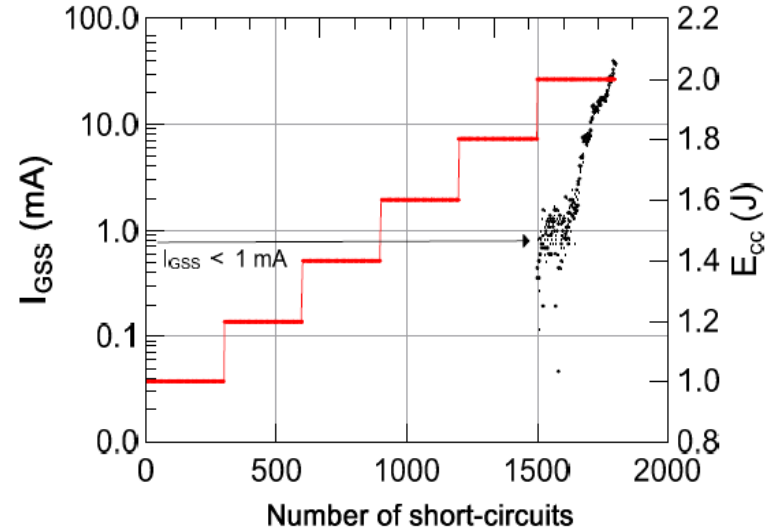
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# Need of reliability insight at semiconductor (die) level



T. Aichinger, et al., Microelectronics Reliability 80 (2018) 68-78.

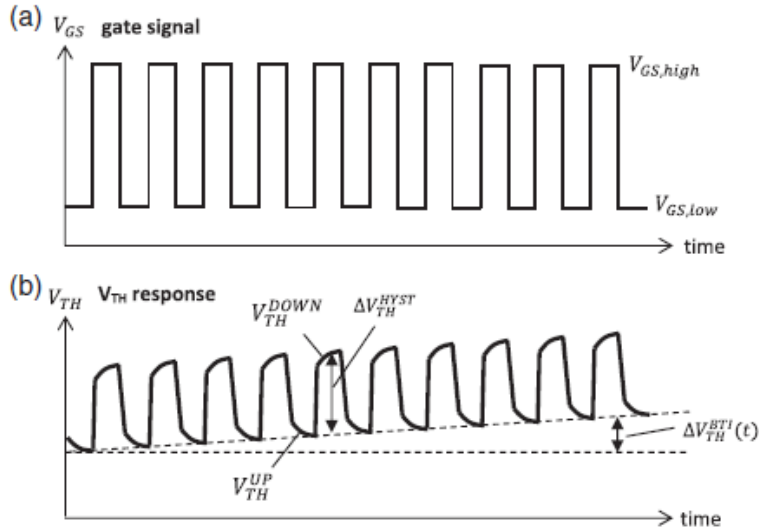


Thèse doctorat. 14/12/2019. Quentin Molin

**How to discriminate between reversible (recovery)  
and not reversible phenomena (aging) !!**

**Lack of SC induced aging indicator !!**

# Need of reliability insight at semiconductor (die) level

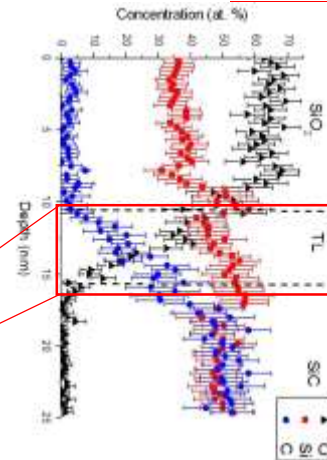
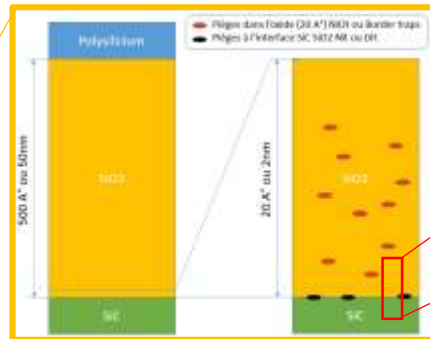
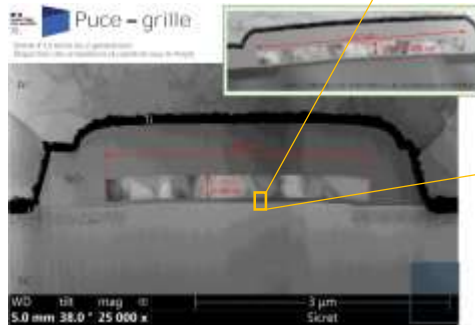


**How to discriminate between reversible (recovery) and not reversible phenomena (aging) !!**

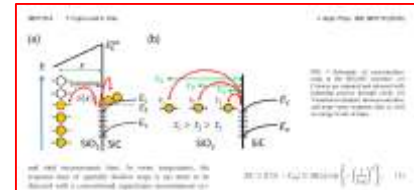
T. Aichinger, et al., Microelectronics Reliability 80 (2018) 68-78.

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**GATE OXIDE RELATED DRIFT:** Causes identification → Focus on the transition layer SiO<sub>2</sub>/SiC



Source: European project (MobiSiC) on Nit improvement by passivation process (N<sub>2</sub>O, NO)



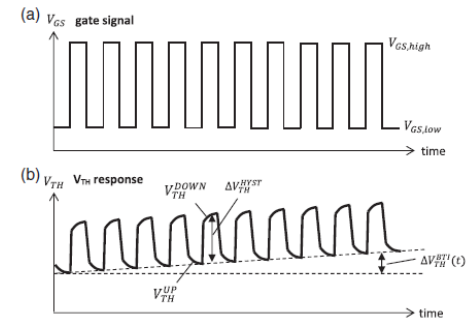
Source: KAKENHI Grant No. 15H03969 (Japan)

Dielectric trap relaxation) → Slow (far from SiO<sub>2</sub>) to Fast (close to SiO<sub>2</sub>)

Background: Existing Patents on gate oxide growth (1/2)

**Patent Number: 5,506,421**  
**Date of Patent: Apr. 9, 1996**  
**Patent No.: US 6,246,076 B1**  
**Date of Patent: Jun. 12, 2001**  
**WO 02/29900 A2 2002**

**The mechanism of defect creation and passivation at the SiC/SiO<sub>2</sub> interface**  
 Peter De'ak<sup>1</sup>, Jan M Knaup<sup>1</sup>, Tam'as Hornos<sup>2</sup>, Christoph Thill<sup>1</sup>, Adam Gal<sup>2</sup> and Thomas Frauenheim<sup>1</sup>  
<sup>1</sup> Bremen 28334, Germany  
<sup>2</sup> Budapest H-1521, Hungary



Source: T. Aichinger, et al., Microelectronics Reliability 80 (2018) 68-78.

# Influence of pre-conditioning on $V_{th}$ measurement

- Currently available SiC MosFET devices present  $V_{th}$  instability.
- Without precaution, the inherent and “normal”  $V_{th}$  instability could blur  $V_{th}$  parameter drift related to device aging.

→ A robust  $V_{th}$  indicator is mandatory for reliability studies.

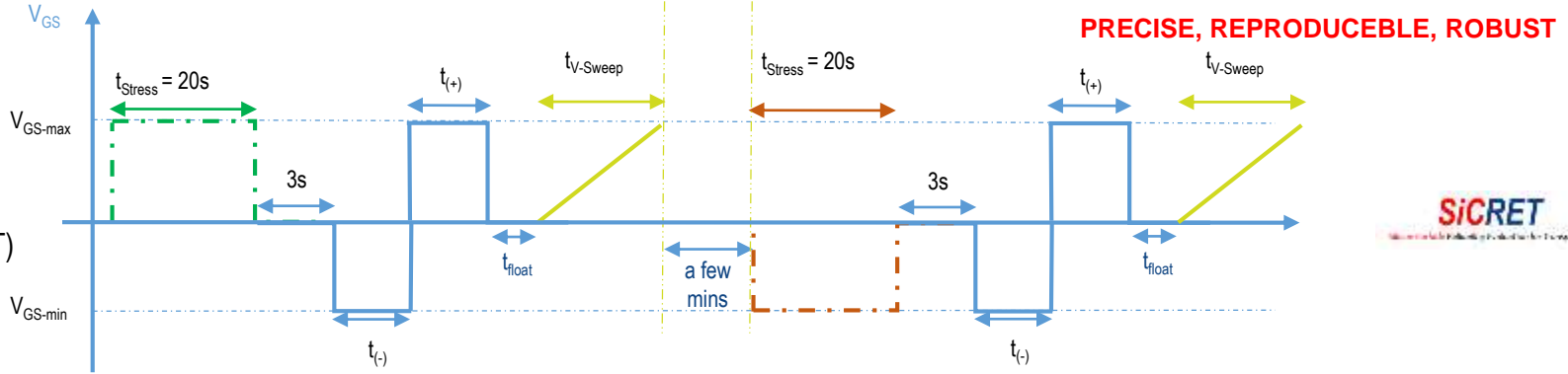
- We have optimized a  $V_{th}$  measurement technique that ensures:
  - independent of previous device normal-operation-history
  - almost perfectly reproducible  $V_{th}$  value, that is based on:
    - device preconditioning-sequence
    - perfect measurements timing-control.
- While standard measurement technique could lead to several hundred of mV  $V_{th}$  instability, depending on previous device operating-conditions, our technique reduces this variation to a few mV range.



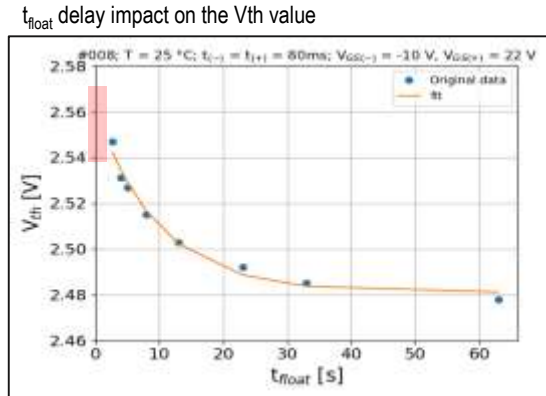
D. Tremouilles

D. Hachem (PD-IRT)

# Influence of pre-conditioning on $V_{th}$ measurement



## ➤ Influence of $T_{float}$



## ➤ Influence of positive / negative stress

Pre-conditioning robustness against device "normal operation history"

Pre-conditioning	$\Delta V_{th-pos}$	$\Delta V_{th-neg}$	$V_{th}$ (V)
Method with $t_{float}=0$	Positive Stress of 20s	Negative Stress of 20s	
Positive only	77 mV	144 mV	3.19
Negative + Positive	1 mV	14 mV	3.15

# Influence of pre-conditioning on $V_{th}$ measurement

## ➤ Open questions

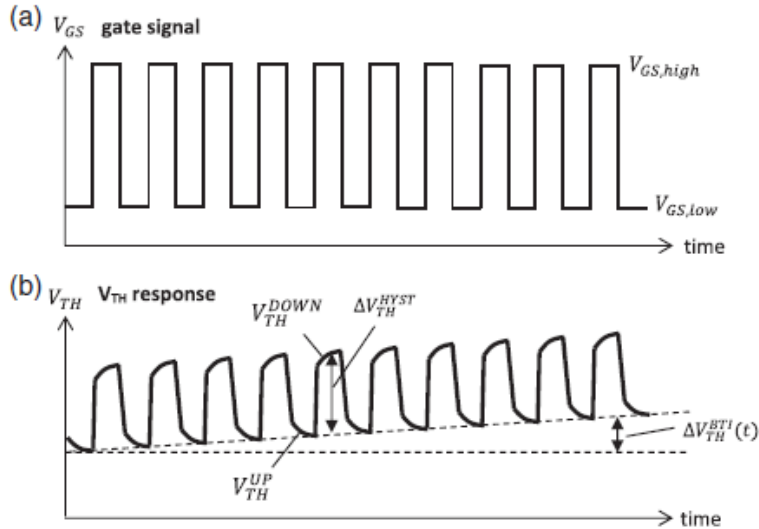
- What is the real  $V_{th}$  behavior during application use case : with switching, with off time,... ?  
What is permanent drift ?  
How hysteresis is evolving during use case ?
- What is impact of  $V_{th}$  variations on conduction ( $R_{DSon}/leakage$ ) and switching losses ?
- How this phenomenon affects behavior of components in parallel or in series?  
Is  $V_{th}$  the proper parameter for selection of components used in parallel?



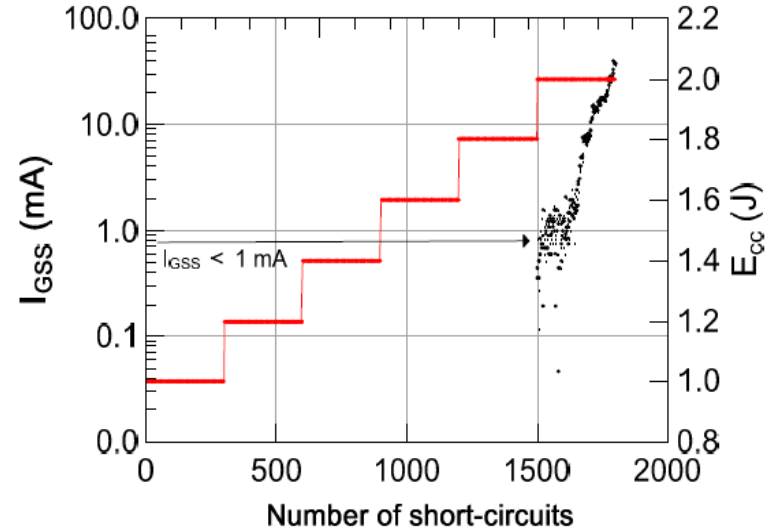
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T. Aichinger, et al., Microelectronics Reliability 80 (2018) 68-78.

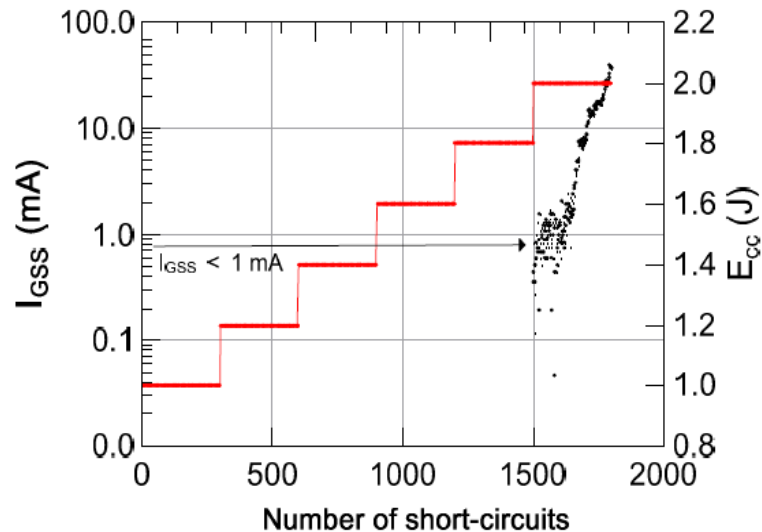


Thèse doctorat. 14/12/2019. Quentin Molin

**Lack of SC induced aging indicator !!**

# Need of reliability insight at semiconductor (die) level

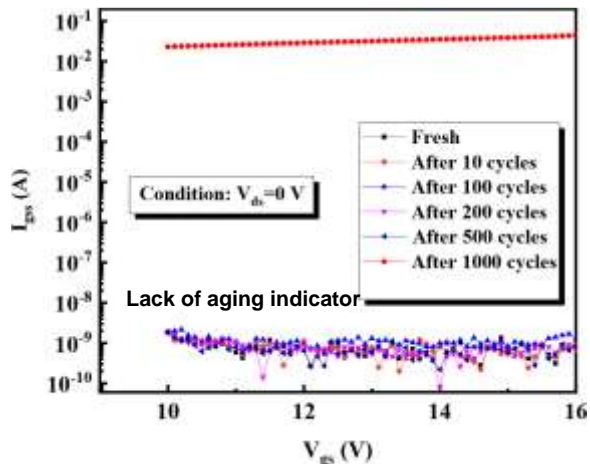
**Lack of SC induced aging  
indicator !!**



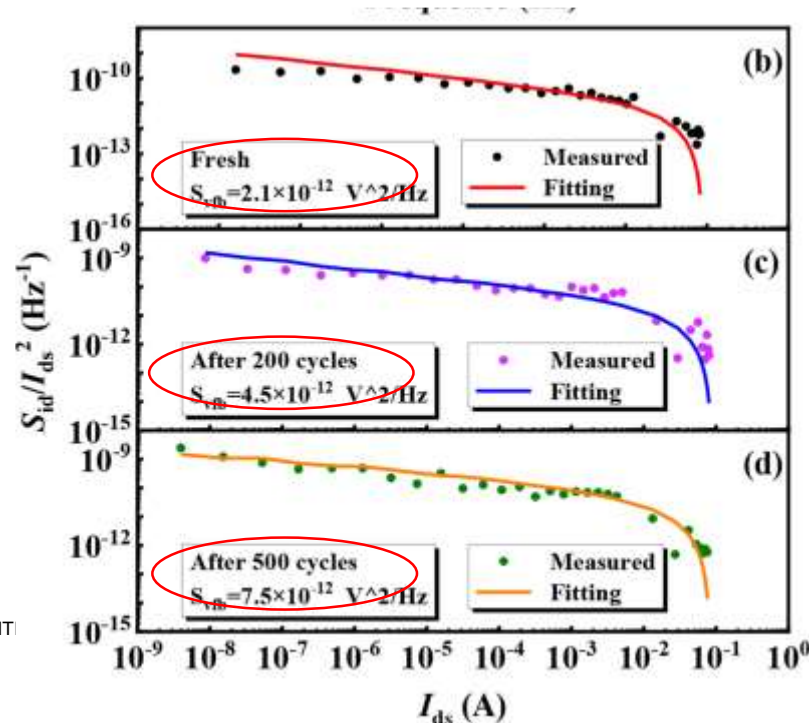
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PRECISE, REPRODUCIBLE, ROBUST

NEED of investigation technique / Approach  
 → LFN based technique !



WANG *et al.*: TRAP ANALYSIS BASED ON LFN FOR SiC pPOWER MOSFETs UNDER REPETITIVE CIRCUIT STRESS



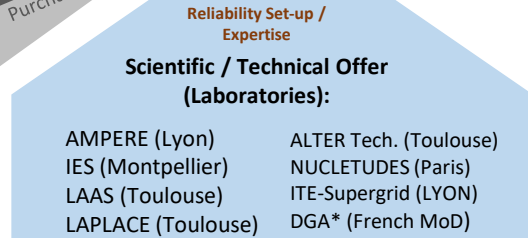
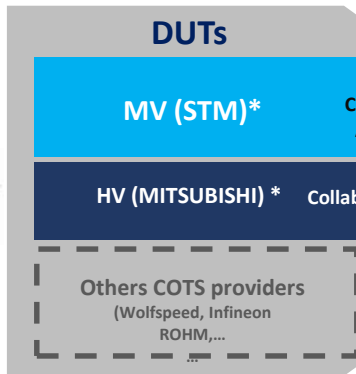
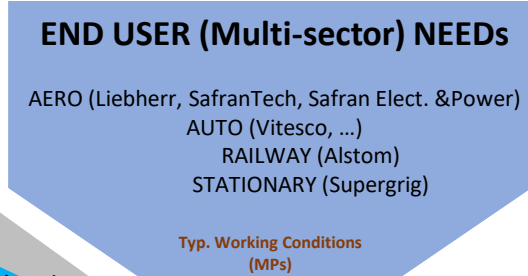
the  $S_{id}/I_{ds}^2$  at 10 Hz versus  $I_{ds}$  for the fresh device, 200 and 500 SC cycles device, respectively.



➤ **Future electrification technologies** will require drastic **improvements of power electronics**, with higher power density & efficiency, but without negative impact on **Reliability**.

➤ **SiC Wide Bang Gap (WBG) technologies** will be **key enablers** thanks to their higher electrical performances (at 1200V toward 3300V)

➤ However **not enough knowledge** and standards test allowing their introduction exist → **High Risks !!!**



afnor

IEC

AEC-Q

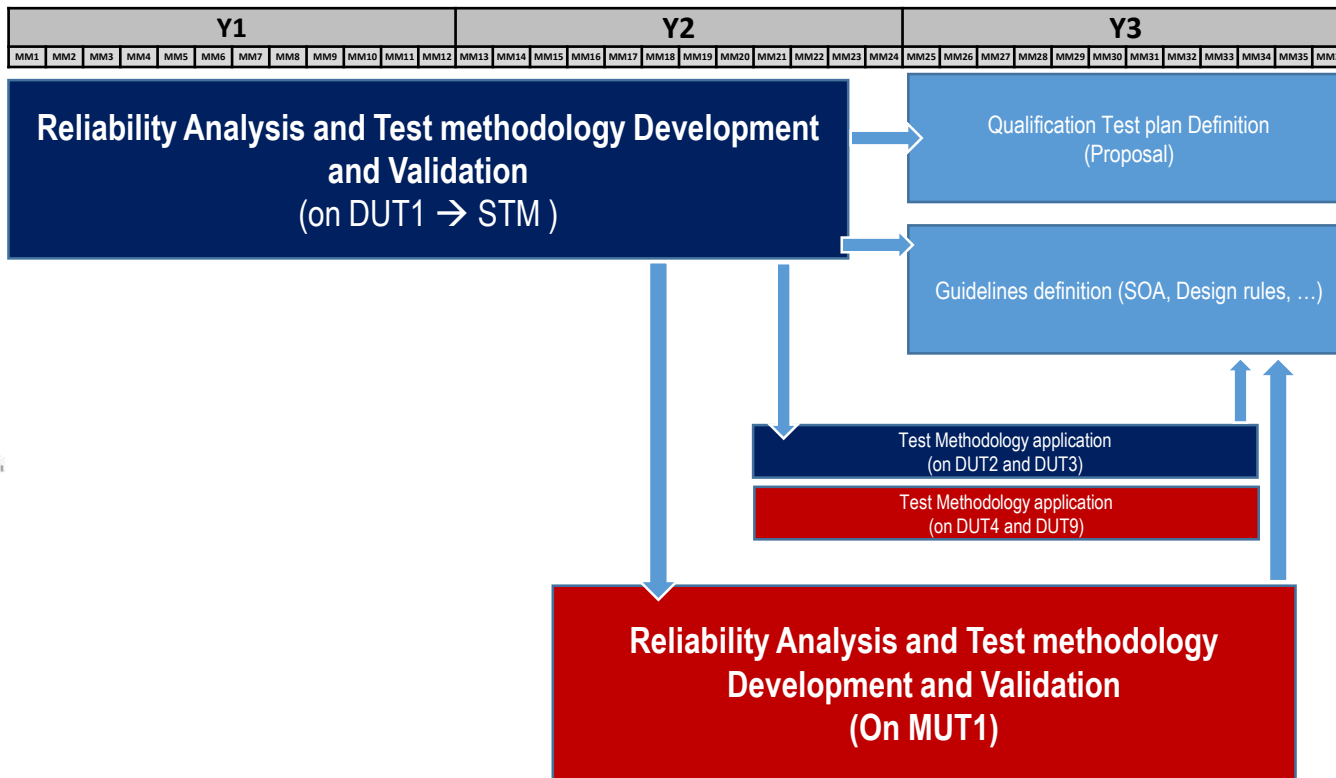
JEDEC



\* Agreement under discussion

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**SICRET**

SICRET

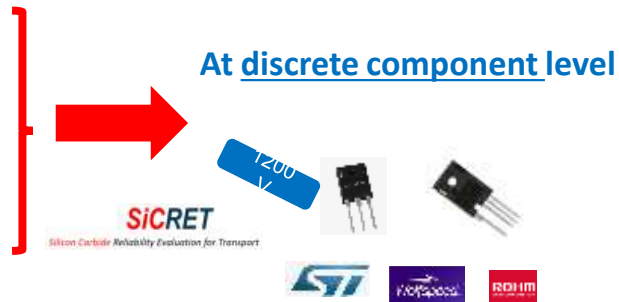
SICRET+

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- Establish a reference body of knowledge (database DUT for Automotive usage profile) of

Qualification Test plan Definition  
(Proposal)

Guidelines definition (SOA, Design rules, ...)



At Power Module level including other studies/tests.

- Low pressure, humidity,
- Thermal management (power cycling, temperature cycling)
- EMC emission/immunity



SiCRET +

⇒ Enhanced by the collaboration with STM  
(associate Partner of the project)



Source: ST Microelectronics





- GaN Wide Bang Gap (WBG) technologies will be key enablers
- However **not enough knowledge NOR “proven-in-use”** and standards test allowing their introduction exist → **High Risks !!!**



# GaNRET

## GaN (Power Transistor) Reliability Evaluation for Transport

Project Set-up Team:



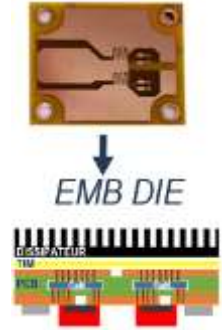
TENTATIVE: BUDGET: **TBD M€** - DURATION: **36MM** Start Date: **2021-Q2**

### ❖ Main Challenges:

- PoF not well understood / established
- Panoply of (not mature) technologies (e/d mode)
- Design rules and test protocol for advanced (embedded) packaging



Source: Schweizer and Infineon



Source: IRT- EPOWERDRIVE Project

### ❖ Application domain:



### ❖ Project Rational:



# Major Challenges wrt SiC

## Lack of standard packaging

### NO-STANDARD PACKAGING (FROM PROPRIETARY TO NO-PACKAGE)



### Difficulty to separate semiconductor and packaging Failure Mechanism

**NO-HIGH-POWER PACKAGING ?**  
(die-size (costs) VS. Perf. (freq., Rds\_on,))  
high-RDS\_on → low die size → high Freq. → Thermal!  
Low RDS\_on → Large die size → low freq → No-Thermal!

### No standard test available\*

\* JEDEC Dynamic High Temperature Operating Life (DHTOL) => JEP189 (Fevrier 2020)

## Many technological choices

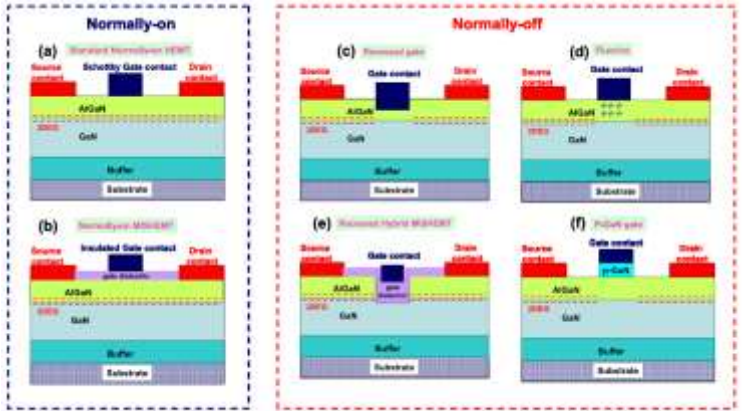


Fig. 5. Schematics of possible configurations for normally-on and normally-off AlGaN/GaN HEMT; left - standard normally-on HEMT layouts with Schottky gate (a) and insulated gate MSHVMT (b); right - normally-off HEMT approaches with recessed gate (c), floating gate (d), recessed hybrid MSHVMT (e) and p-GaN gate (f).

### POWER GAN SUPPLY CHAIN & BUSINESS MODEL

Color	Category
Red	Substrate/Carrier
Orange	Gate/Drain/Source Contact
Yellow	AlGaN/GaN/AlN Epitaxial Layers
Green	AlN Buffer Layer
Blue	SiC Substrate

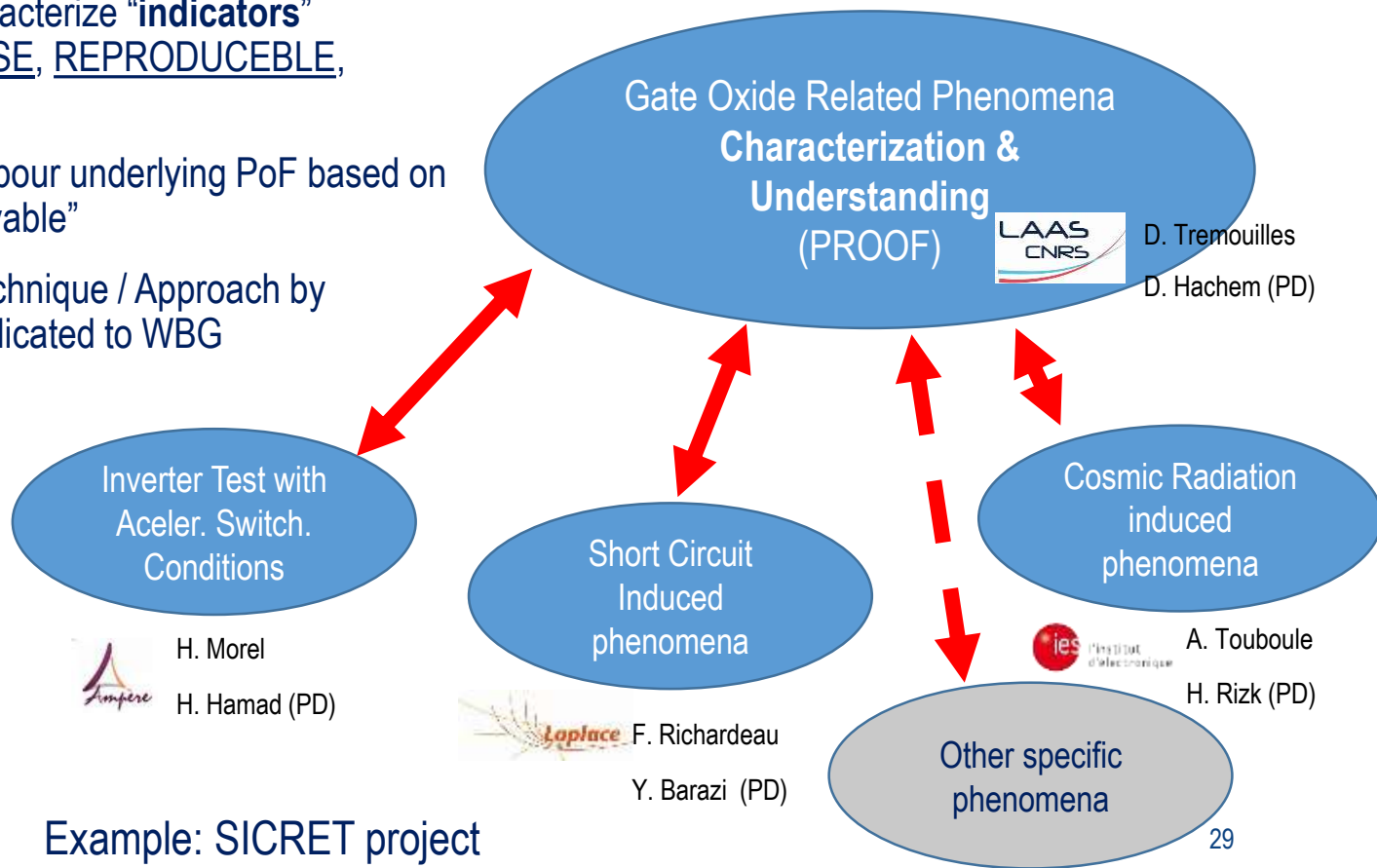


The landscape is populated by many providers (SME often fables) using large foundries with established Silicon legacy !

# Exploitation and Lighthouse Activities

- **Consolidation** of a reliability and risk assessment tool (capitalization)
- **Structuring** National reliability network (CFF, NRTW, ...)
- **Supporting** international standardization (JEDEC, EIC, JEITA, ...)
- **Connecting** with major international players/networks (AEC, ECPE, CPES, ...)

- Need to identify and characterize “**indicators**” **observables**” by PRECISE, REPRODUCIBLE, ROBUST methods
- Need to understanding about underlying PoF based on above “indicators” observable”
- NEED of investigation technique / Approach by specialized platforms dedicated to WBG



Example: SICRET project



# Acknowledgements

**Project:**

*ePowerdrive, Integration, Feline, SiCRET*





Merci de votre attention

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