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Dynamic RDS-on degradation analysis on power GaN HEMT by means of TCAD simulations and experimental measurement

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Introduction – GaN HEMTs for power electronics

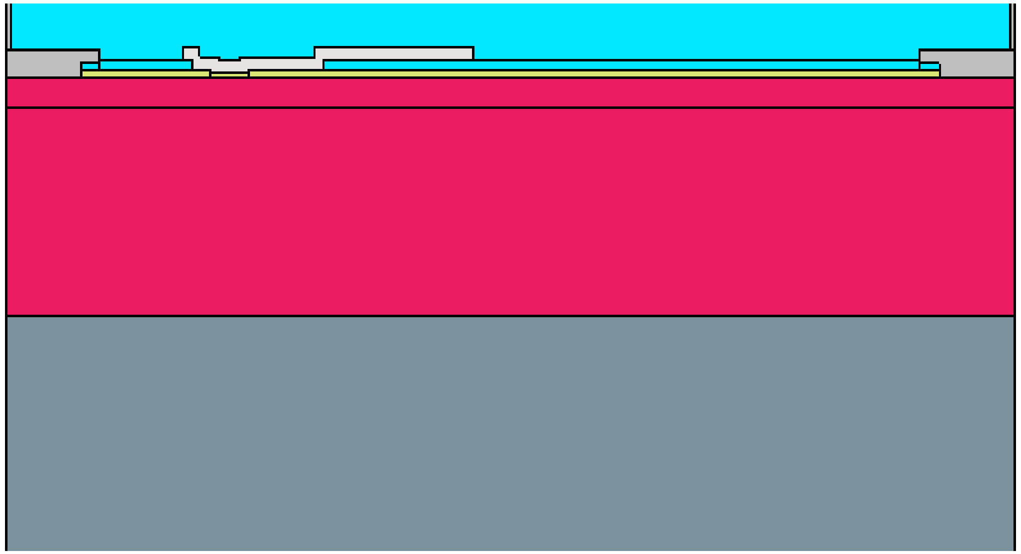
GaN HEMT widely adopted for power application thanks to:

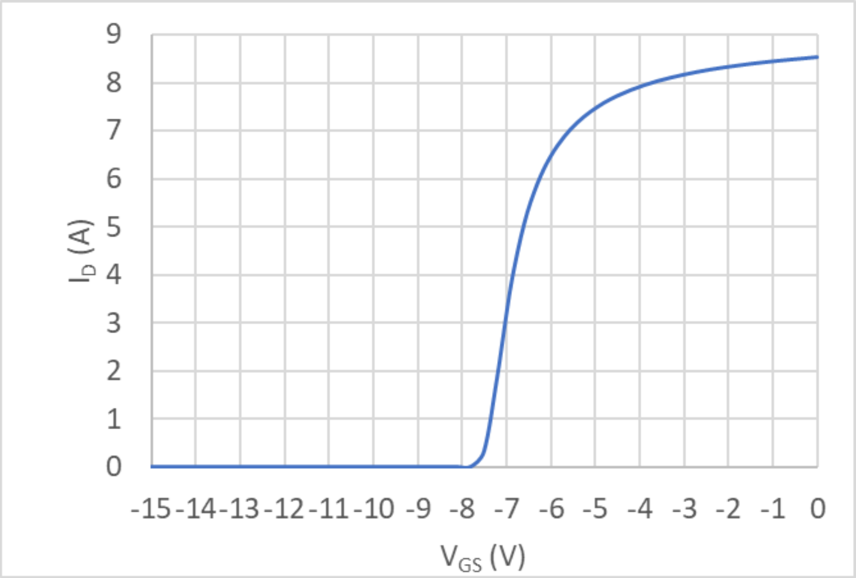
- ✓ high critical electric field → high voltage
- ✓ high 2DEG mobility and concentration → low $R_{DS\text{-}on}$

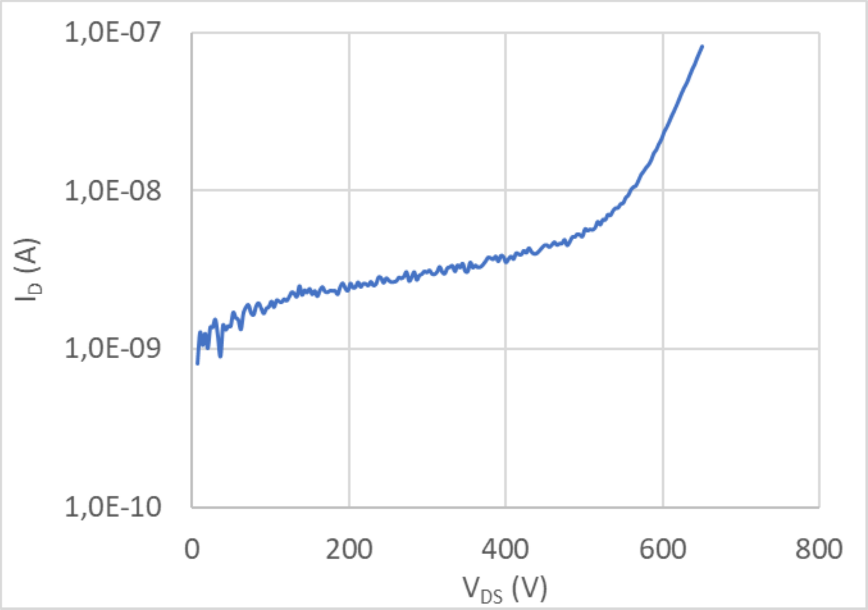
However, GaN technology still present reliability issues:

- ✓ For high voltage Fe or C is mandatory to limit leakage current → creation of point defect traps related to these species
- ✓ Deep trap levels lead to current collapse effect → electrical performance degradation

Transistor technology under test

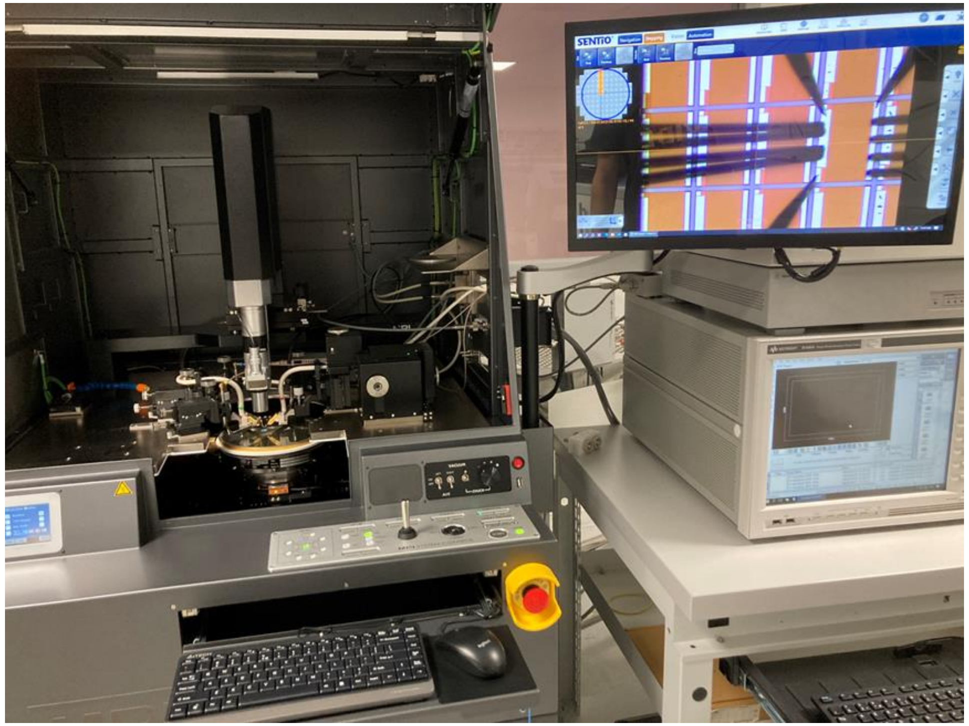


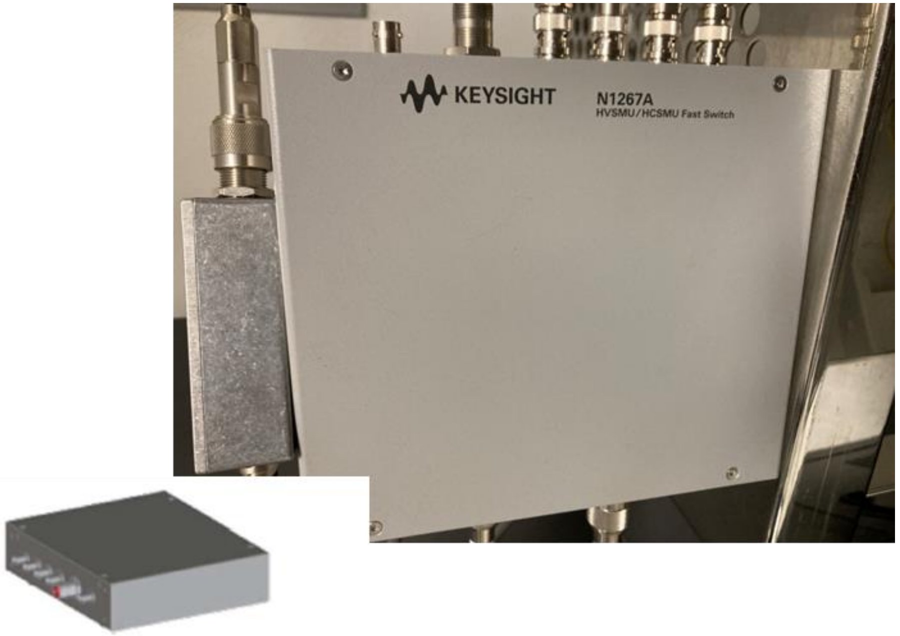




- D-mode power HEMT for 650V applications
- Carbon doped buffer on Si substrate 8 (inches)
- Three field plates design

Experimental setup

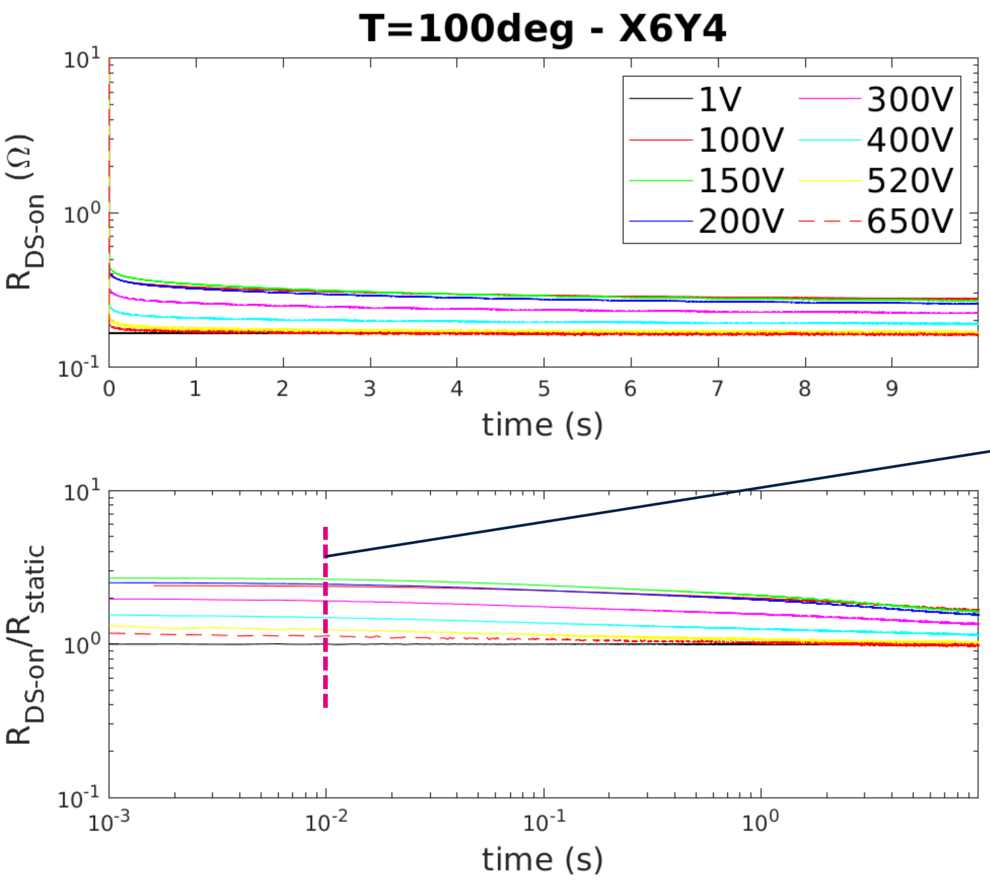


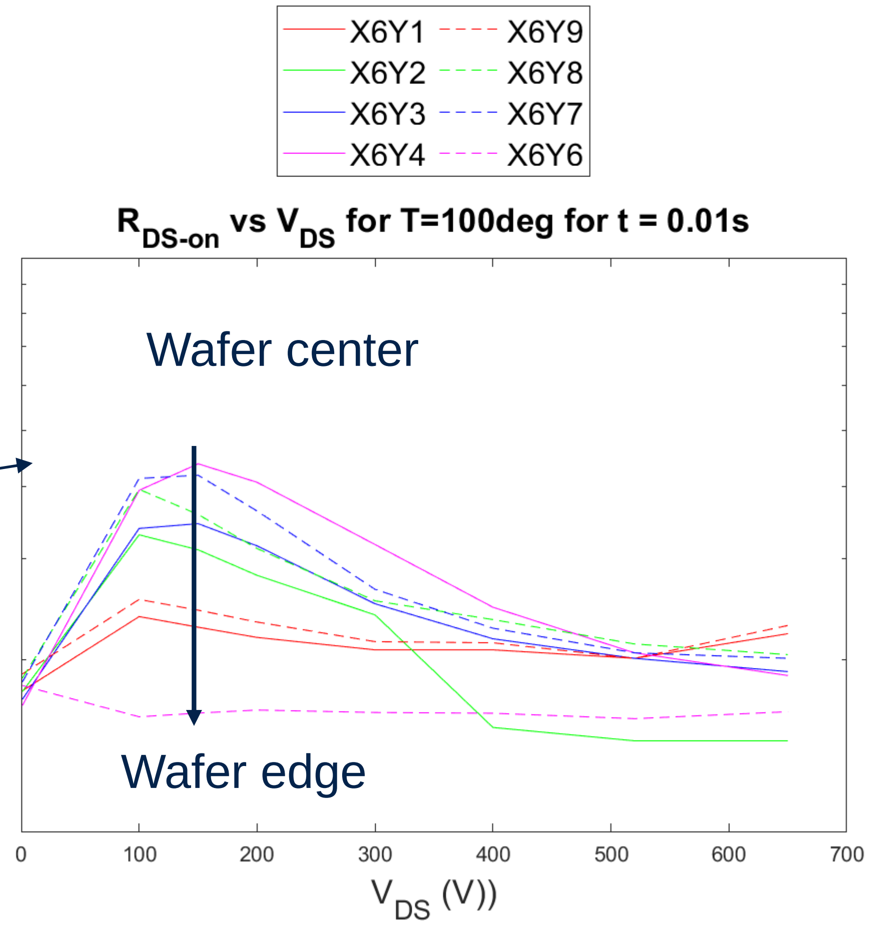


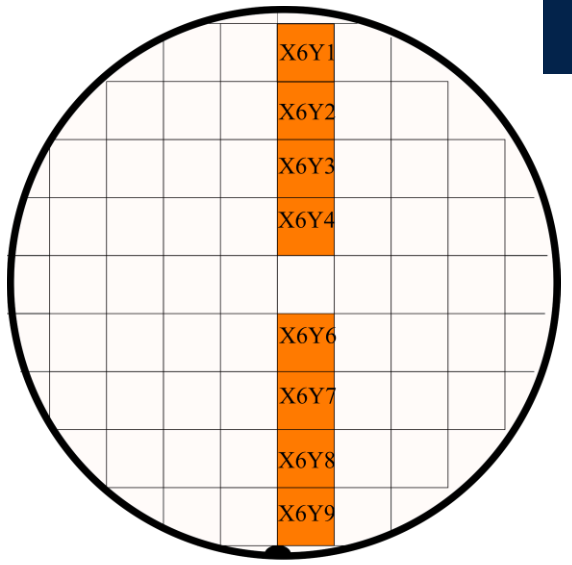
N1267A High Voltage / High Current Fast Switch

- Characterizations performed with B1505 associated to the and semi automatic probing station
- Current collapse option (high voltage / high current fast switch) to monitor $R_{DS\text{-}on}$ variation after a stress
- Test performed on power transistors for different conditions:
  - Stress time: 1min
  - V_{DS} (100 to 650V)
  - Temperatures between 80 and 120°C

Measurement results

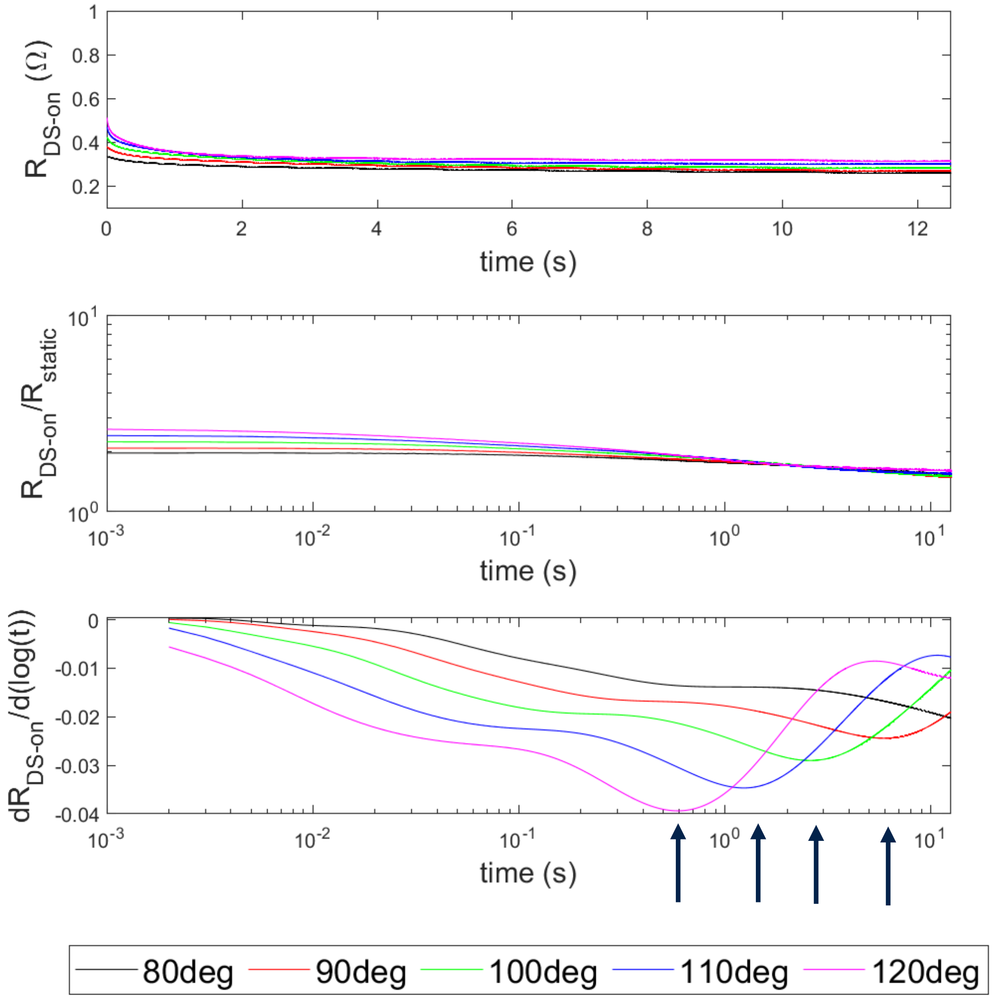


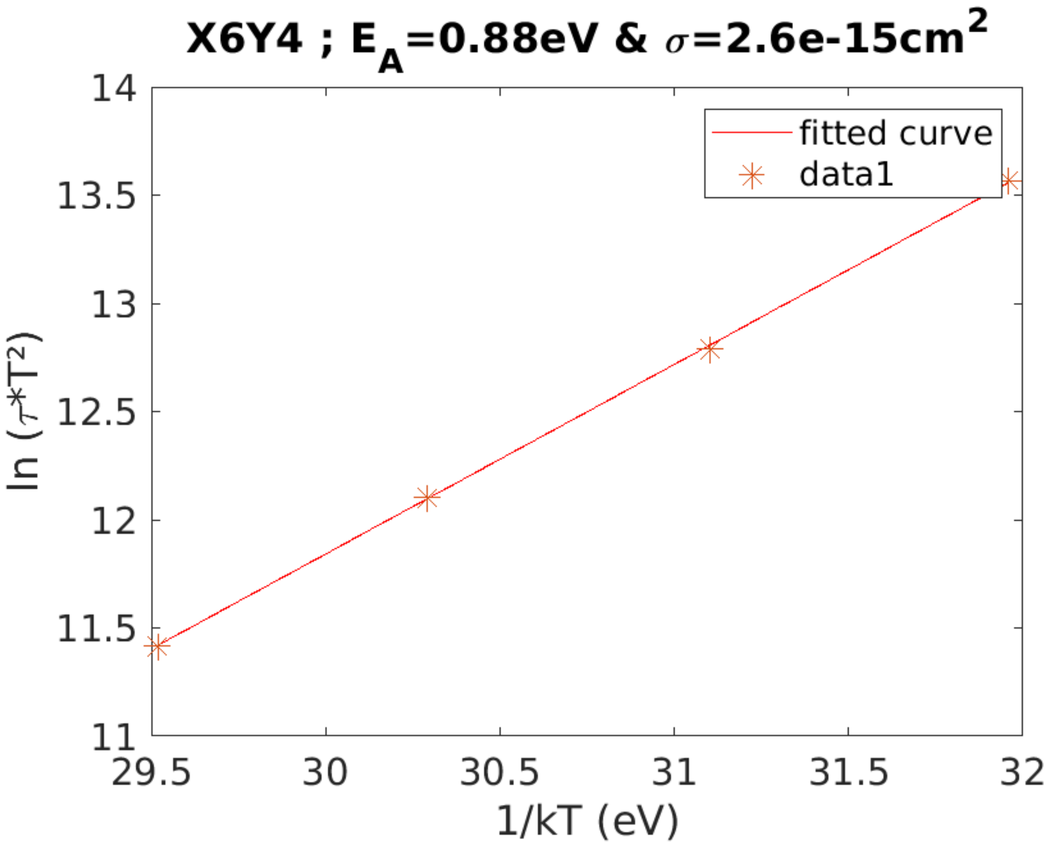




- **Stress voltage effect:** Maximum of degradation for low V_{DS} (100-150V), with a decrease at higher voltage
- **Center to edge effect:** Stronger degradation in the center of the wafer
- Symmetry effect on wafer position: same degradation at left and right from center

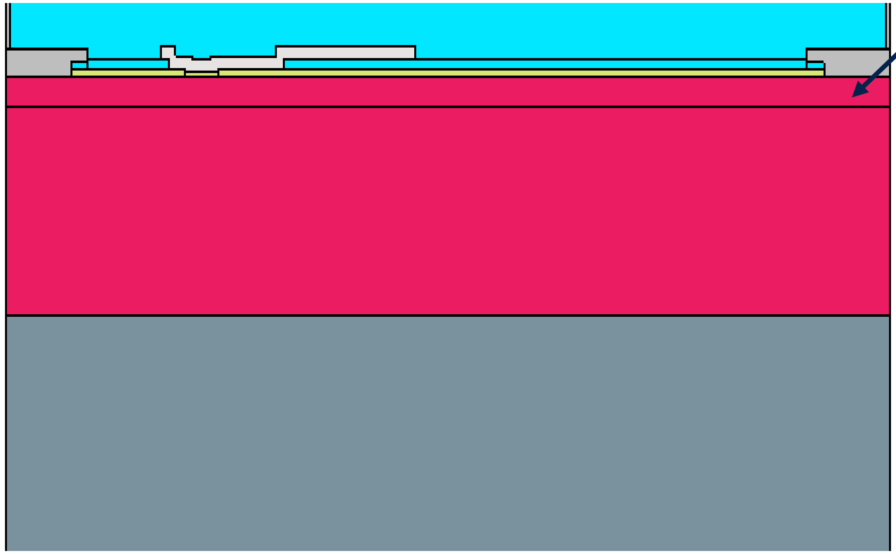
Measurement results

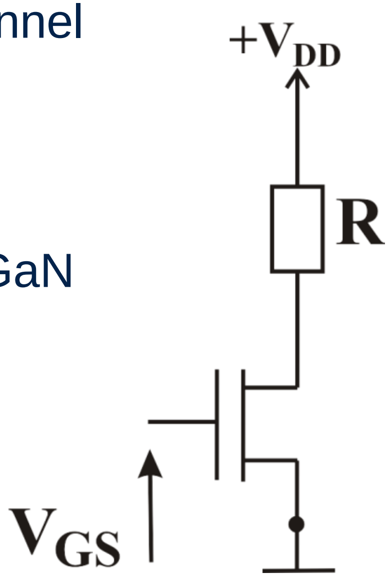


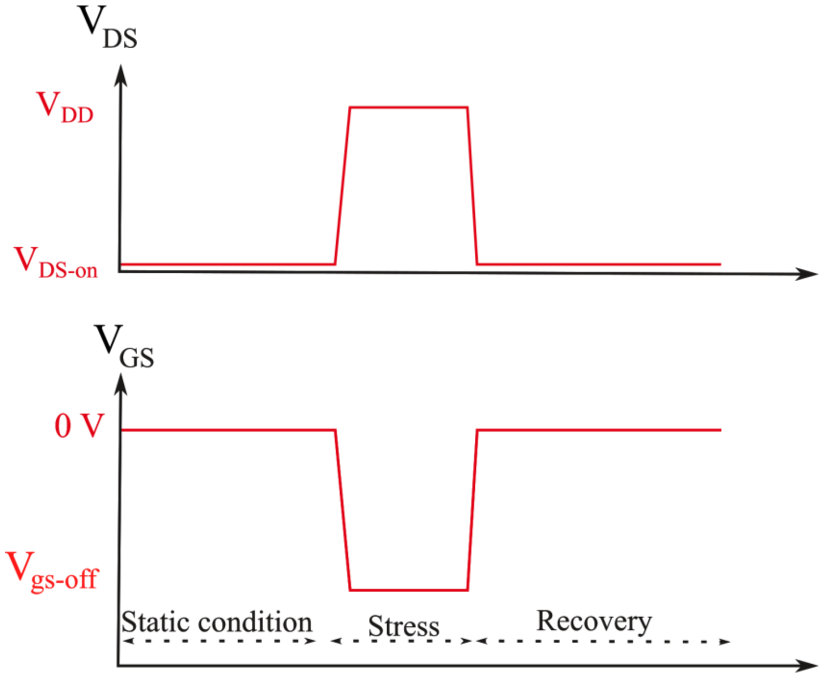


- Test repeated at different temperature for the most stressful condition: 100V in the center of the wafer
- Main trap time constant extracted from derivative of $R_{DS\text{-}on}$
- Activation energy E_A=0.88eV: should be associated to carbon used in the epitaxy

Simulation conditions

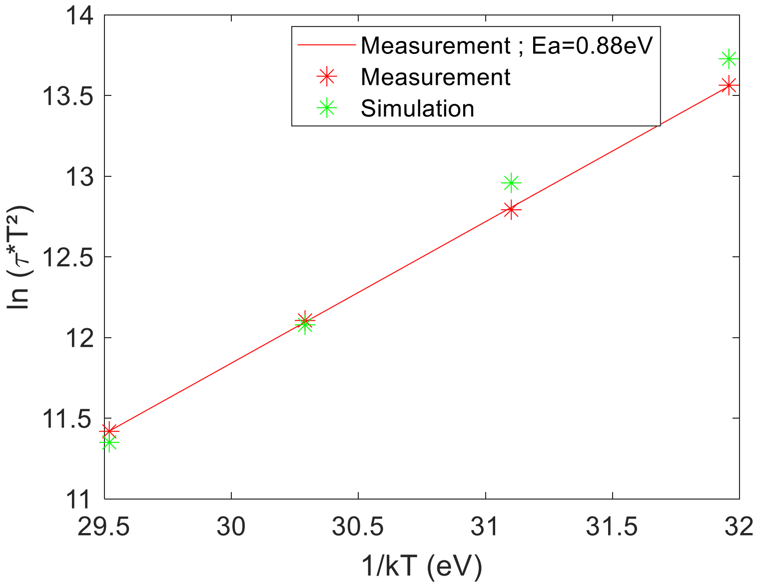




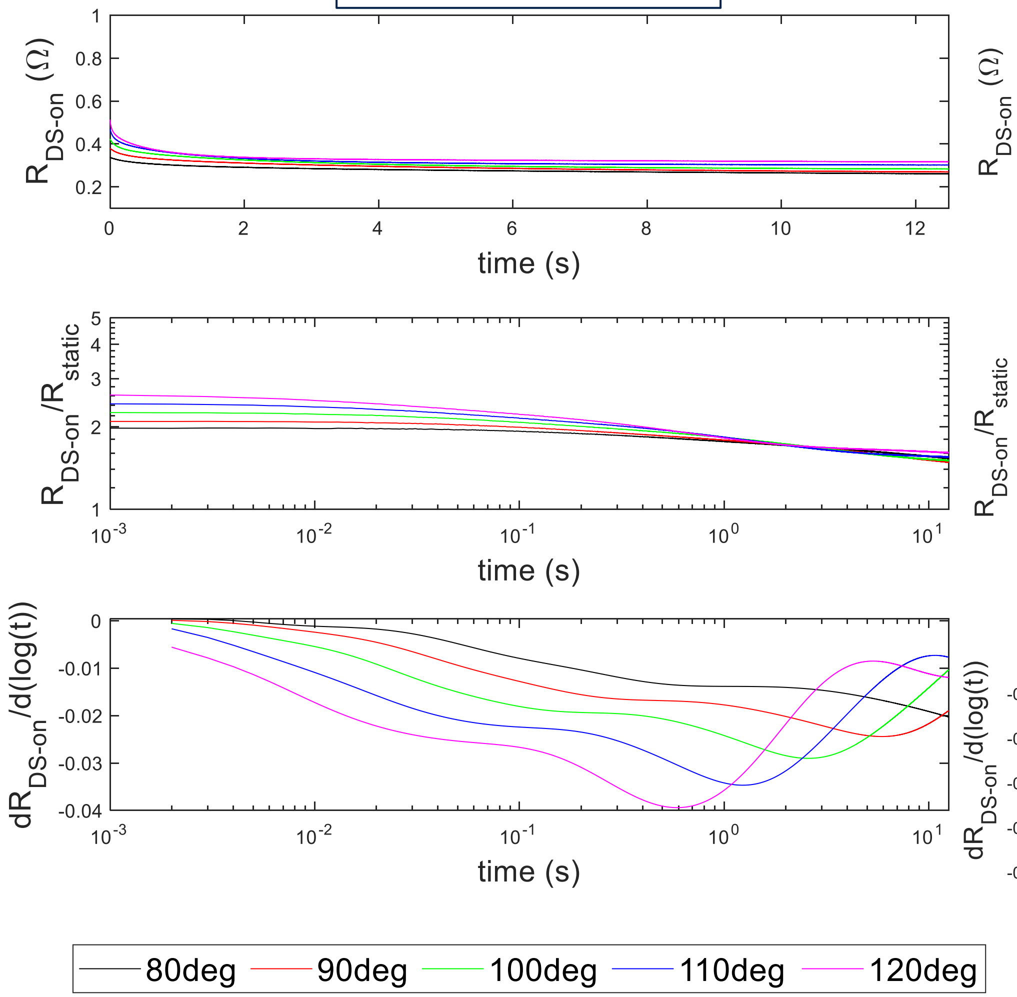


- Mixed mode simulation
- Resistor value selected in order to limit the drain current to 1A (HEMT in linear mode)
- Pulsed source used for the gate with $V_{gs\text{-}off}$=-30V with very fast rise / fall time in the range of ns
- Buffer modelized by GaN associated to acceptors traps (E_T=0.9-E_V)
- Lower concentration of acceptors in the GaN channel, fully compensated by shallow donors
- General physical parameters:
  - Piezo-electric polarization based on Ambacher model
  - SRH recombination for traps
  - Mobility: temperature dependance due to phonon scattering & Canali for high field saturation

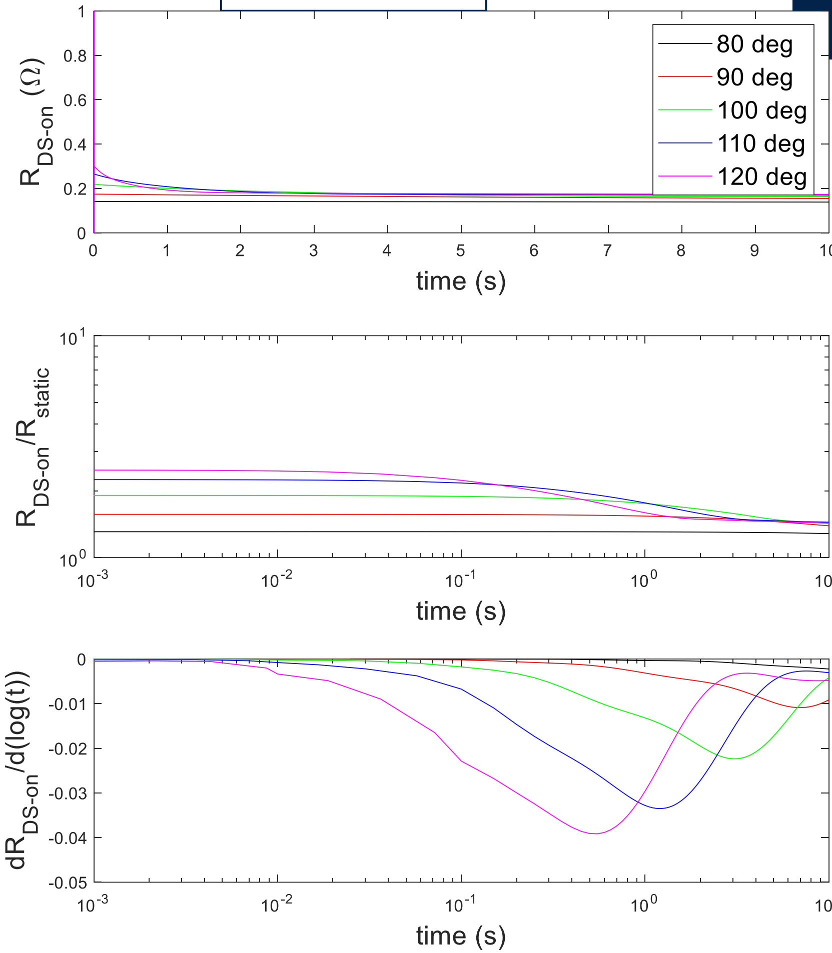
Impact of temperature – tests on new wafer



Measurement



Simulation



<u>Stress conditions</u>

- V_{DS}=100V; V_{GS}=-30V
- Stress duration: 1min

- Time constant dependent on trap cross section
- Same trends in terms of $R_{DS\text{-}on}$ variation in simulation by adjusting the acceptor concentration
- Activation energy of ~0.9eV extracted from TCAD results

Conclusion

- Dynamic $R_{DS\text{-}on}$ variation measured on D-mode HEMT for different condition highlighted the stronger degradation at low voltage

- Low voltage stress for different temperatures allowed us to extract an activation energy of 0.9eV that could be related to carbon

- TCAD simulation with traps of same activation energy in the GaN buffer could reproduce the same trend and allowed us to understand the electrical behavior

- Thanks to TCAD simulations, we could improve the transistor design to mitigate the $R_{DS\text{-}on}$ degradation.

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