Building confidence in SiC and GaN technologies: PROOF's role in IRT collaborative projects

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Fabio Coccetti
IRT Saint Exupéry (Toulouse)

fabio.coccetti@irt-saintexupery.com

www.irt-saintexupery.com

CONTEXT & MOTIVATION

The main vector to enable energy transition is ELECTRIFICATION of systems and functions!

Main challenges

- ***Function Densification***

  → *Densification* ***KW/Liter - KW/Kg***

  → *Efficiency* ***(reducing losses) > 95%***

  by 2 main levers

  - ***Wide Band Gap Power Electronics !***
  - ***High Voltage (current) !***

- ***Functional Safety*** *(Dependability)*

Safety ***- Reliability – Availability – Maintainability*** *— (Testability - Reparability – Confidentiality – Integrity – Certificability)*

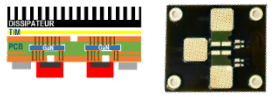
→ ***CONFIDENCE*** *in the underlying technology !*

Technological & Methodological Levers

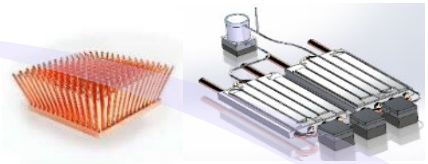
The big picture toward Electrification

Optimized Control

WBG Power Module Integration

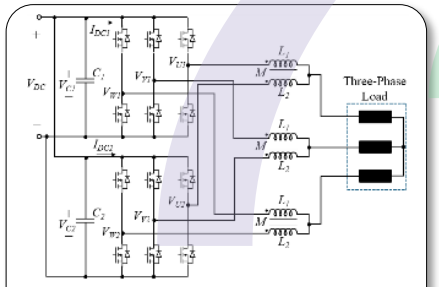


WBG PCB embedded

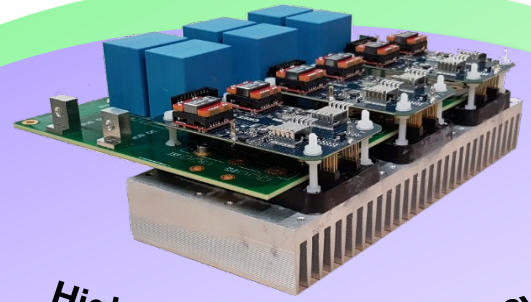


Thermal modeling and testing (Zth)
Cooling Systems

Magnetics
(machine and tarnsf.)

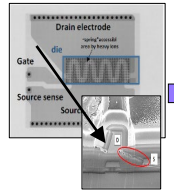


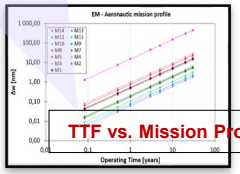
Converter Topology



High Integration & Efficiency

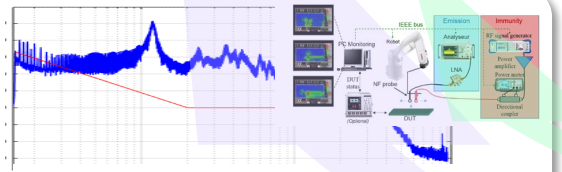
High Dependability (harsh Envir / High constrain)





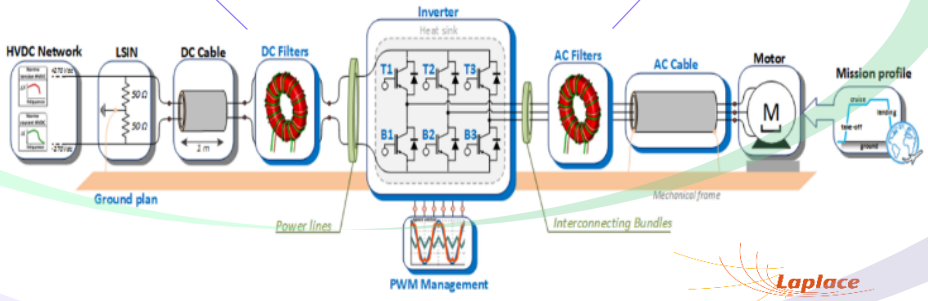
Failure Risk Assessment Methodology

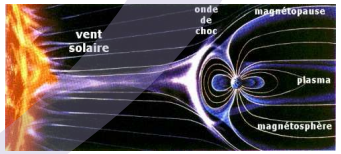
RF Design and Modeling



HF, EMC/I from component to system
(active filter, Near field Scanning, …)

Multidisciplinary Analysis / Optimization / Validation





Cosmic radiation Immunity

In-System-Validation

Testing and Optimizing the converter in the entire EM chain

Technological & Methodological Levers

The big picture

Performance DENSIFICATION !

Power density, efficiency, ….

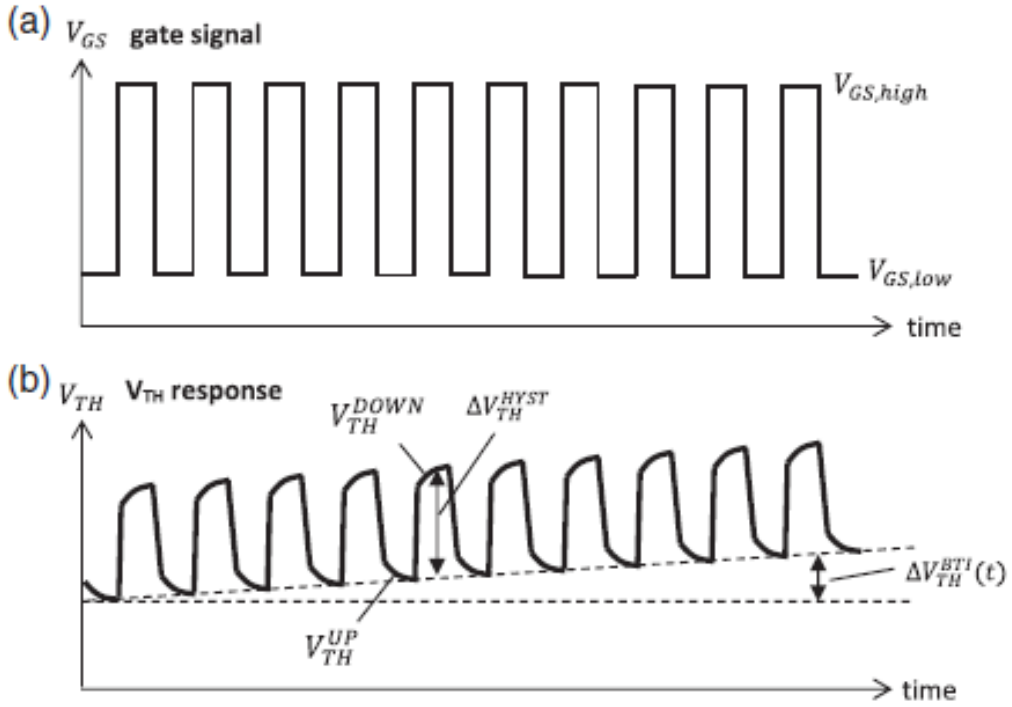
CONFIDENCE in Design and Use !

Margin Aware Design and Use RULES!

EXPLICABLE !

Provide the underlying Physics (of Failure, of working)

Need of reliability insight
at semiconductor (die) level



T. Aichinger, et al., Microelectronics Reliability 80 (2018) 68-78.

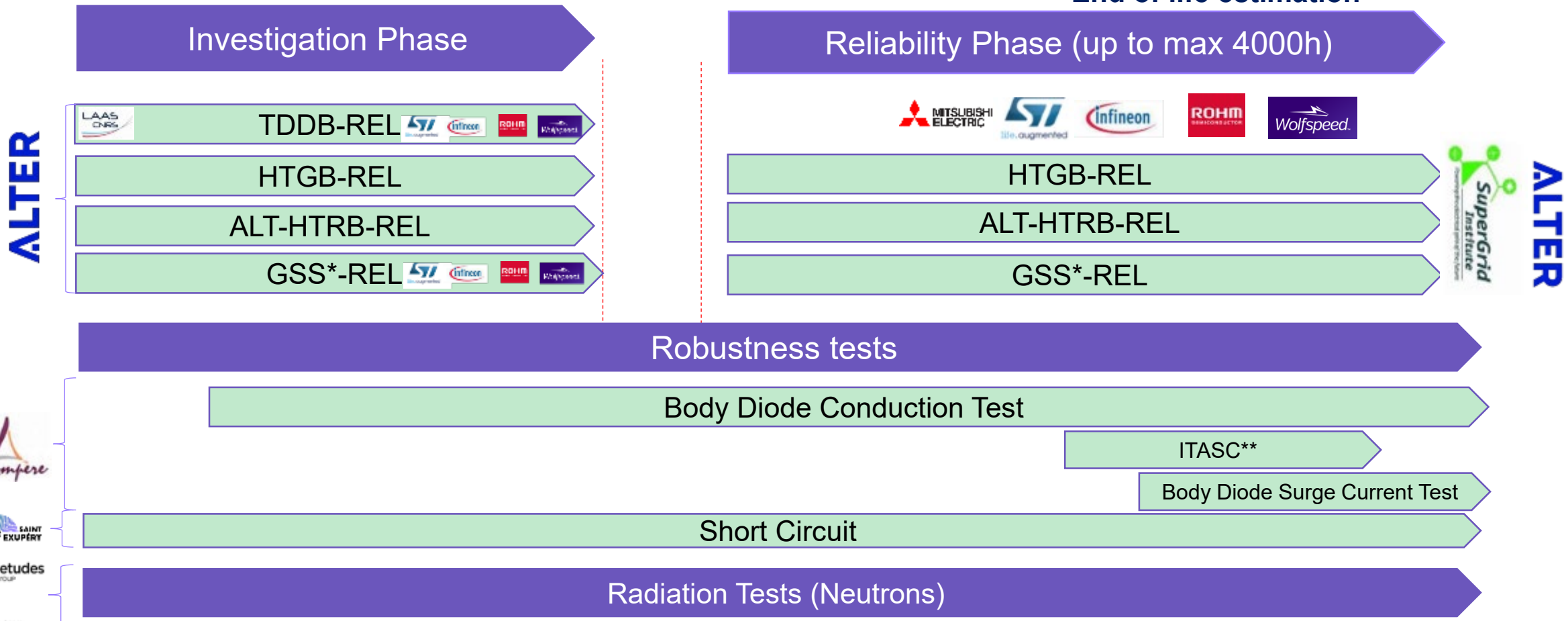
How to discriminate between reversible (recovery) and not reversible phenomena (aging) !!

Reliability Methodology

Optimal Approach toward costs-effective test of SiC MOSFET

Investigation phase: Main Stressor definition

Reliability phase: Aging models
End of life estimation

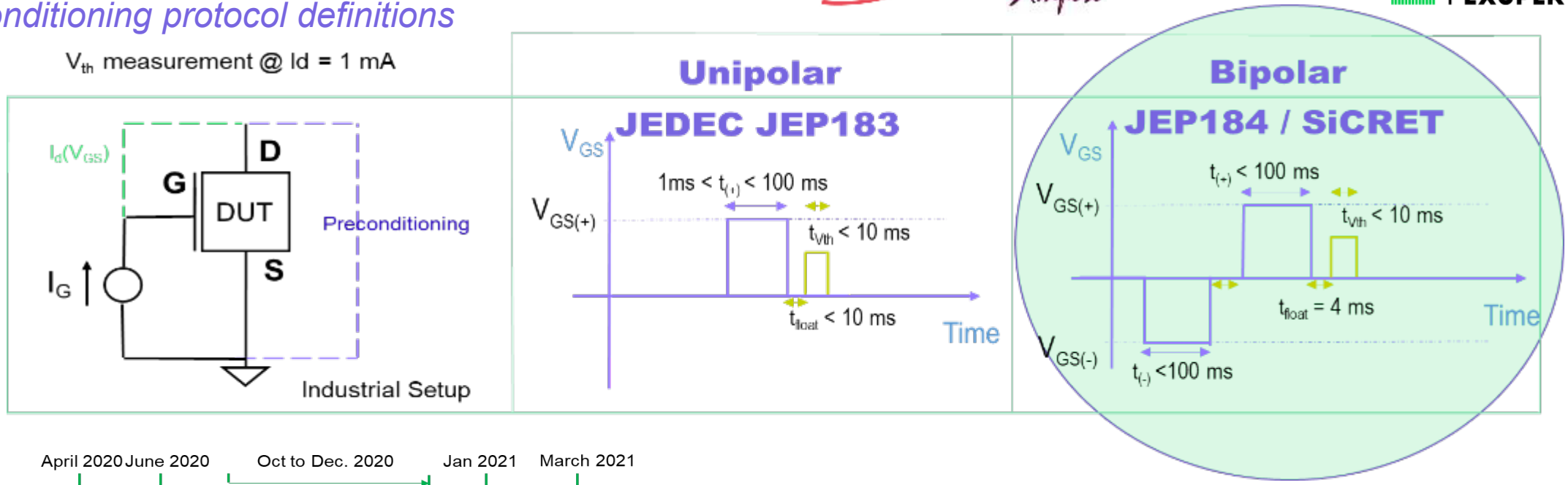


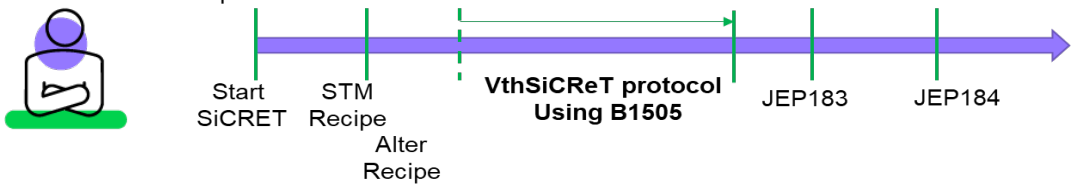
* Gate Switching Stress (See JEP195)
**Inverter Test with Accelerate Switching Condition

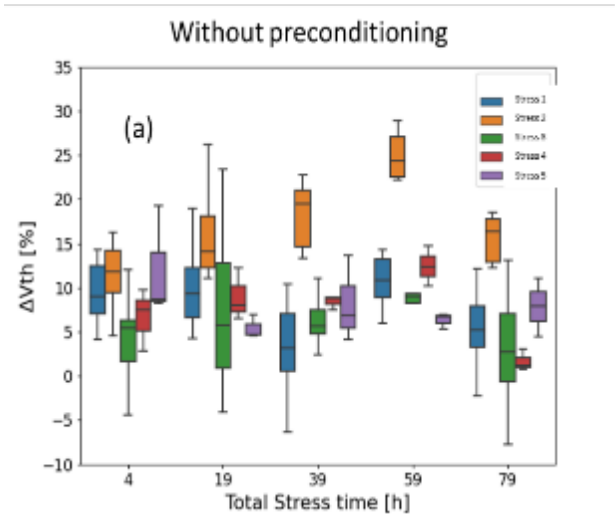
« REL » → above usual qualification time, up to EoL or degradation to derive ageing law

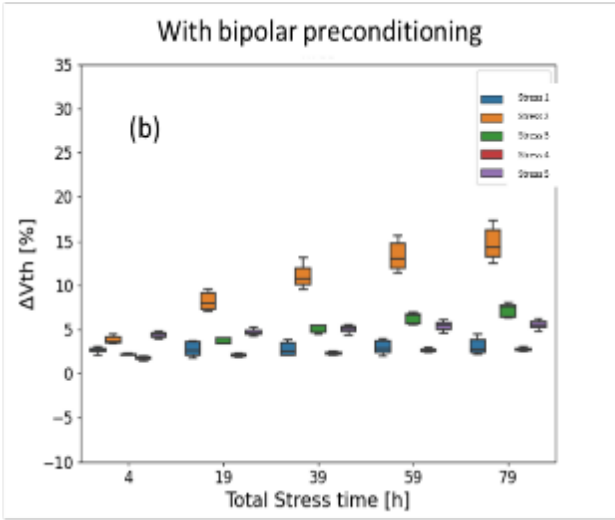
Vth Characterization for SiC MOSFET

Preconditioning protocol definitions









Bipolar Vth Preconditioning protocol:

→ Since December 2020 (Prior to Jedec standard JEP183)
→ In collaboration with Alter, Ampere, LAAS laboratory.
→ Very stable and Robust
→ Main aging indicator

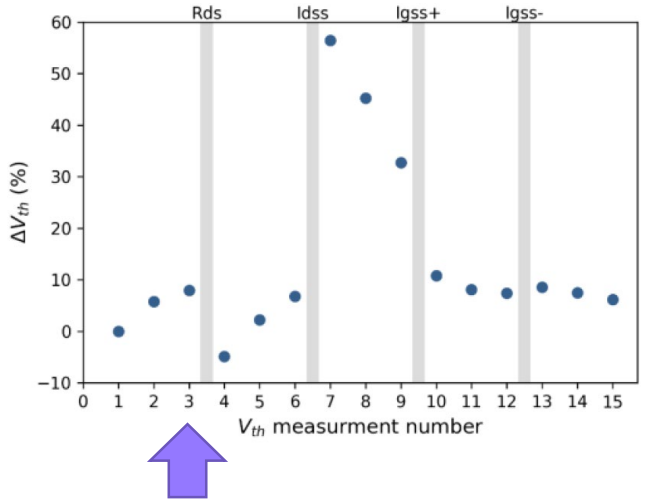
David TREMOUILLES - Dani HACHEM (2021-2022)
SICRET Project

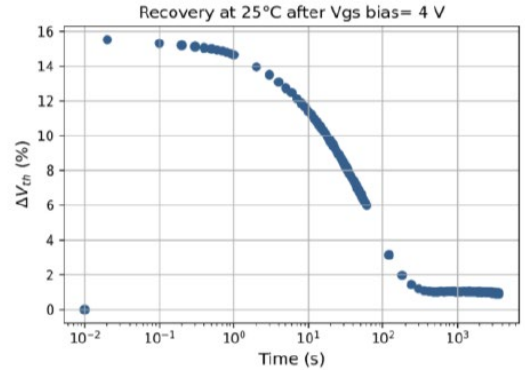
Vth Characterization for Power GaN HEMT

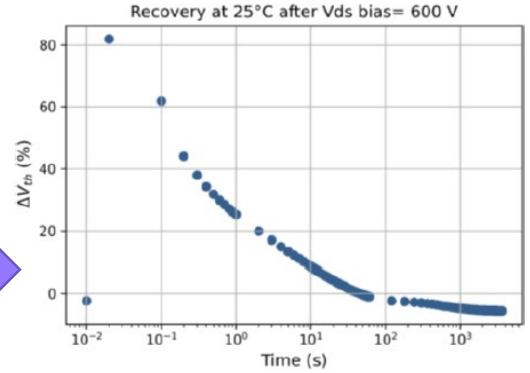
Preconditioning protocol definitions

Vth Preconditioning protocol:

→ NOT unique: Dipends from providers, Technology, …
→ JEDEC not yet dealing with this issue
→ Methodology to choose it has been defined

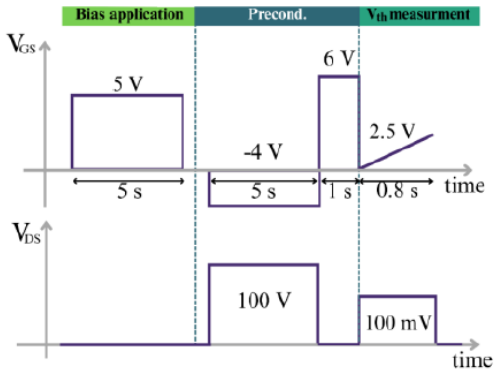


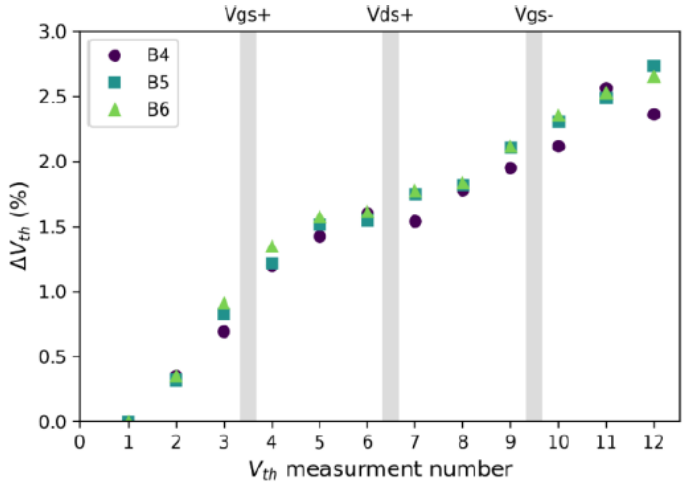




Variation of the threshold voltage after *different types of characterization* and *in time*

Vth temporary elevation is recoverable and reverts to its original state after few hundreds of seconds.





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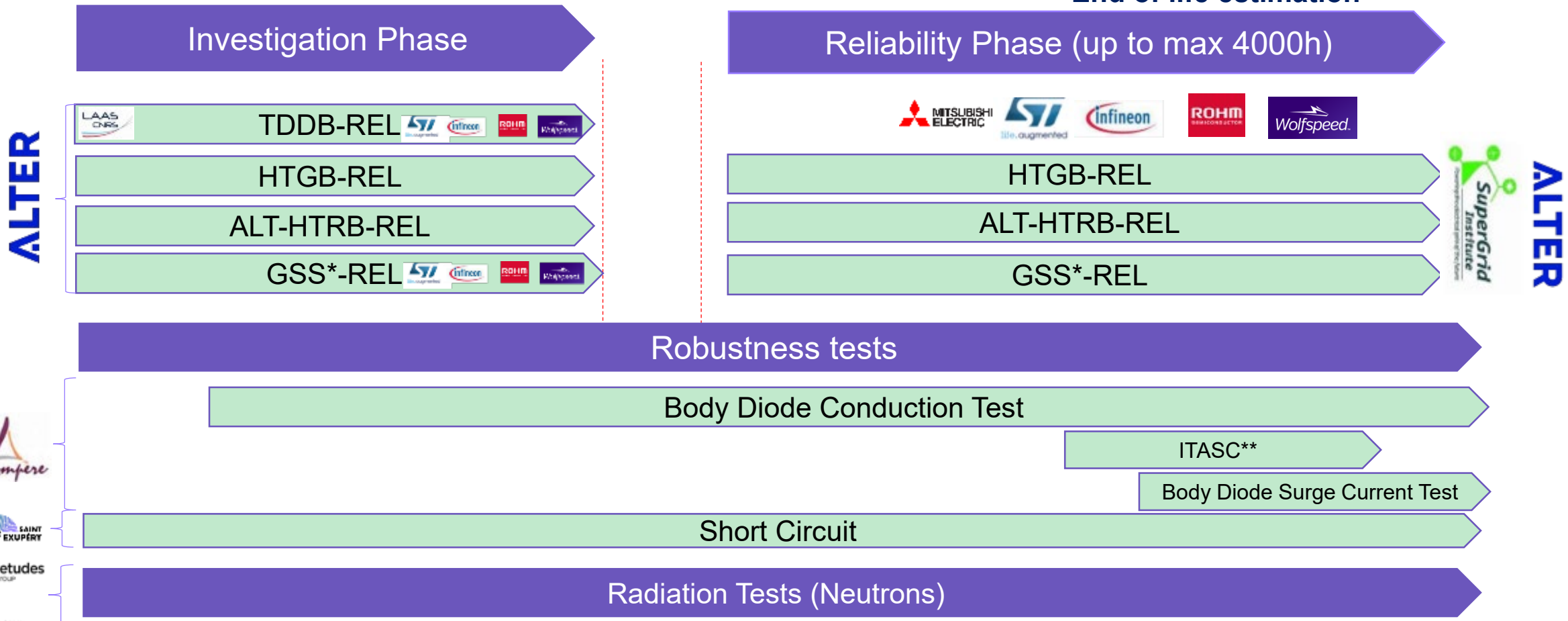
David TREMOUILLES – Maroun ALAM (2023 – 20xx)
GANRET Porject

Reliability Methodology

Optimal Approach toward costs-effective test of SiC MOSFET

Investigation phase: Main Stressor definition

Reliability phase: Aging models
End of life estimation

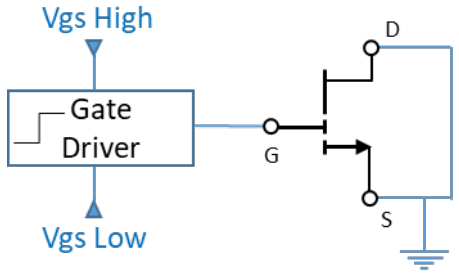


* Gate Switching Stress (See JEP195)
**Inverter Test with Accelerate Switching Condition

« REL » → above usual qualification time, up to EoL or degradation to derive ageing law

HTGS → GSS test conditions – Screening DOE

Same DoE for each Manufacturer



HTGS DoE	Gate voltage	Temperature	Frequency	Duty cycle	Qty
Condition 1	Vgs,off / Vgs,on	25°C	500 kHz	20%	3
Condition 2	VgsMin /Vgs,on	25°C	500 kHz	20%	3
Condition 3	VgsMin / VgsMax	25°C	500 kHz	20%	3
Condition 4	Vgs,off / Vgs,on	25°C	500 kHz	80% (*)	3
Condition 5	VgsMin / Vgs,on	25°C	500 kHz	80% (*)	3
Condition 6	Vgs,off / Vgs,on	125°C	500 kHz	20%	3
Condition 7	VgsMin / VgsMax	125°C	500 kHz	20%	3
Condition 8	Vgs,off / Vgs,on	175°C	500 kHz	20%	3
Condition 9	VgsMin / Vgs,on	175°C	500 kHz	20%	3
Condition 10	VgsMin / VgsMax	175°C	500 kHz	20%	3
Condition 11	Vgs,off / VgsMax	175°C	500 kHz	20%	3
Condition 12	VgsAv / Vgs,on	175°C	500 kHz	20%	3

Device Selection:

- Trench and Planar technologies
  - DUT A: Trench
  - DUT B: Planar
  - DUT C: Trench
  - DUT D: Planar
- Last SiC Mosfet generation available in 2020/2022
- TO-247-3L package
- Automotive Grade version
- Range caliber: 1200V, ~30 A, ~75 mΩ

Glossary (from datasheet):

- Vgs,on: Recommended turn-on gate voltage
- Vgs,off: Recommended turn-off gate voltage
- VgMax: Max positive transient voltage
- VgMin: Min negative transient voltage
- VgsAv: Average value between VgsMin and Vgs,OFF

JEDEC GSS – JEP195

Investigation Test duration: 85h (1.53E+11 cycles)
Remote interim Readouts: 4h, 23h, 45h, 65h

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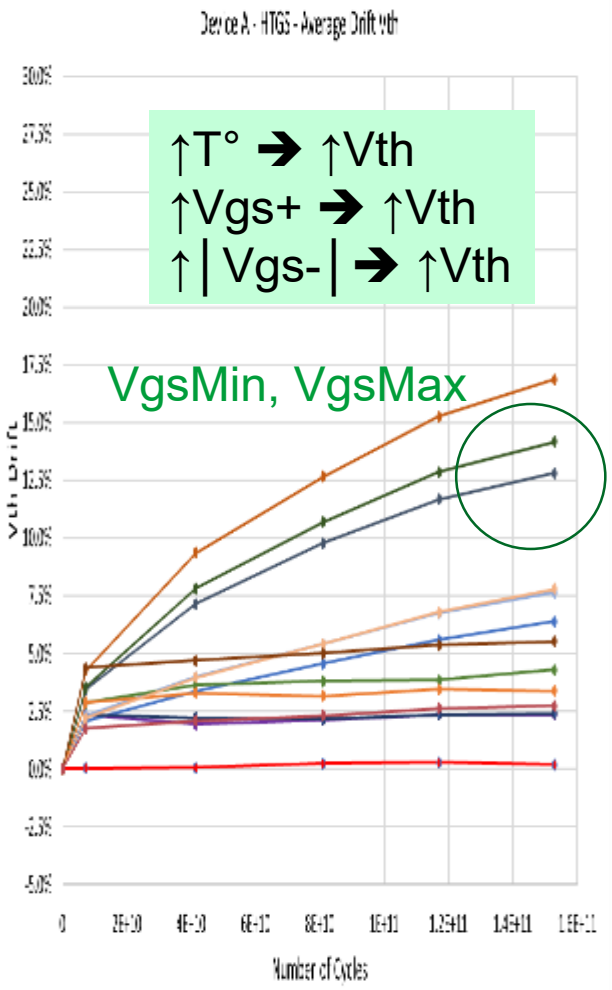
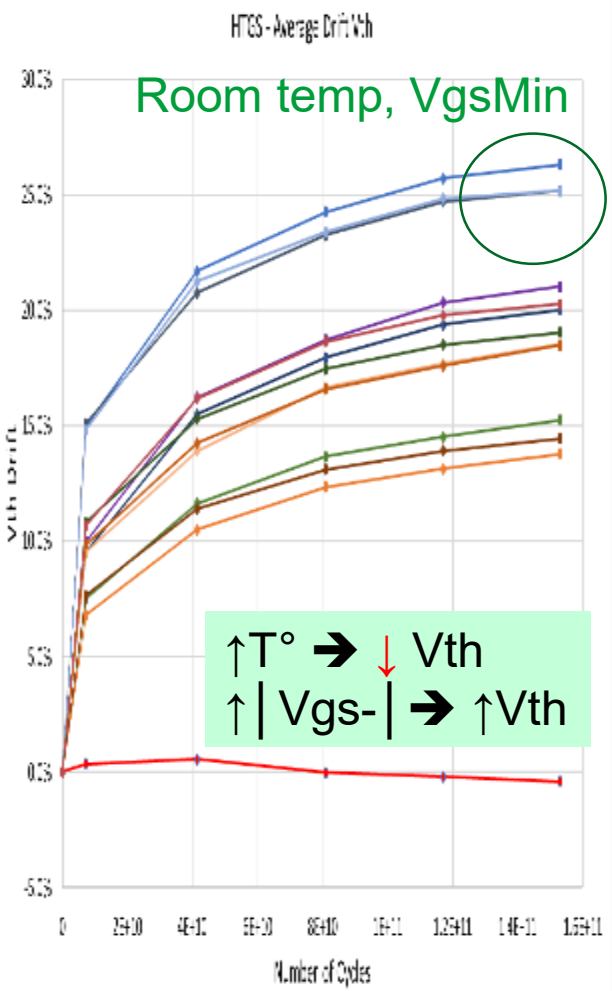
DC parameters used as indicator: $V_{GS(th)}$, $R_{DS(ON)}$, VHyst, BVDSS, Vsd, Idss, Igss, Cgs, LFN, Switching Energy

HTGS→ GSS : Vth (1mA) drift

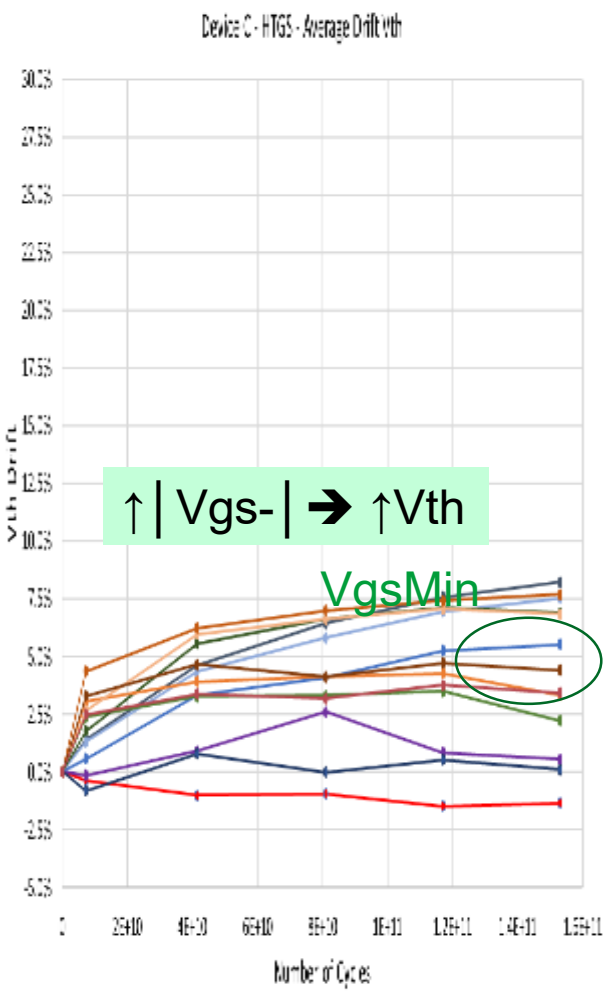
DUT A – Trench



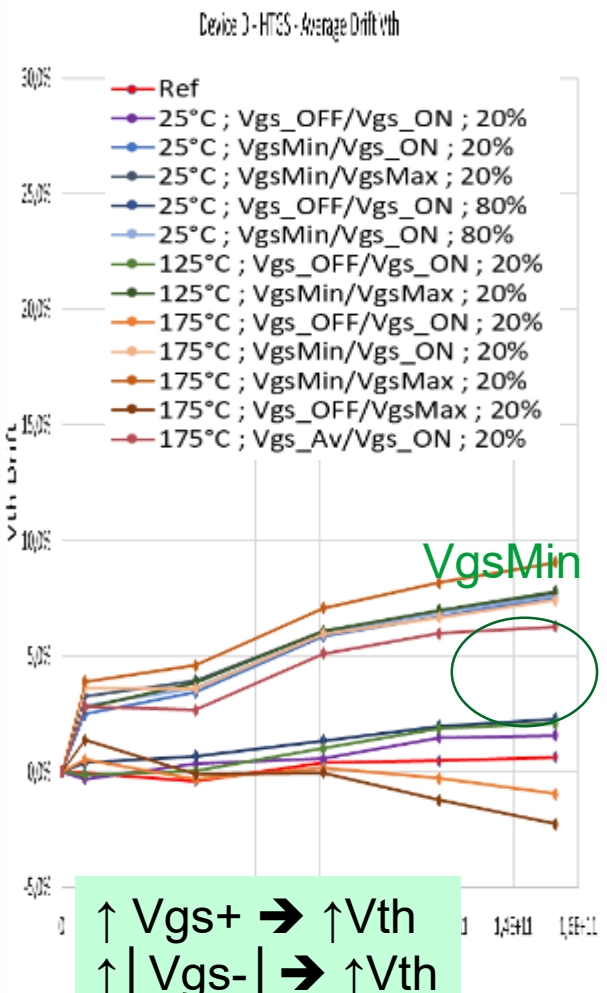
DUT B - Planar



DUT C - Trench



DUT D - Planar



Main stressors are technology dependent

Reliability Methodology

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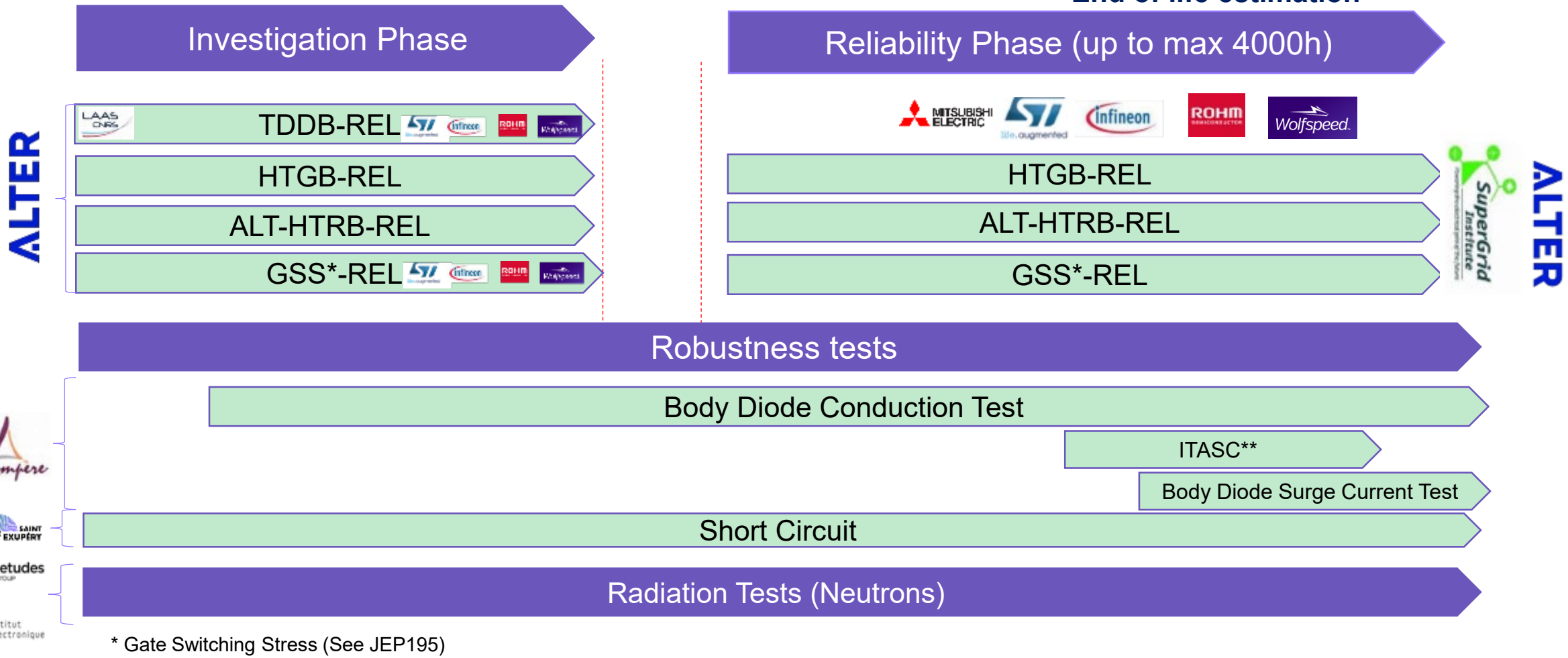

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**Inverter Test with Accelerate Switching Condition

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Reliability Model Extraction for Lifetime Prediction

Vth degradation model under GSS for planar and trench technologies

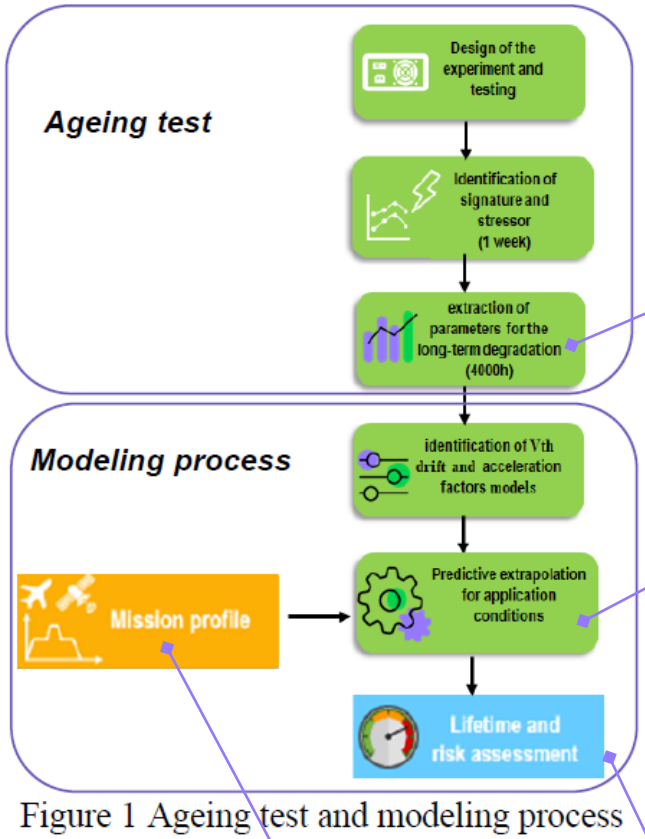
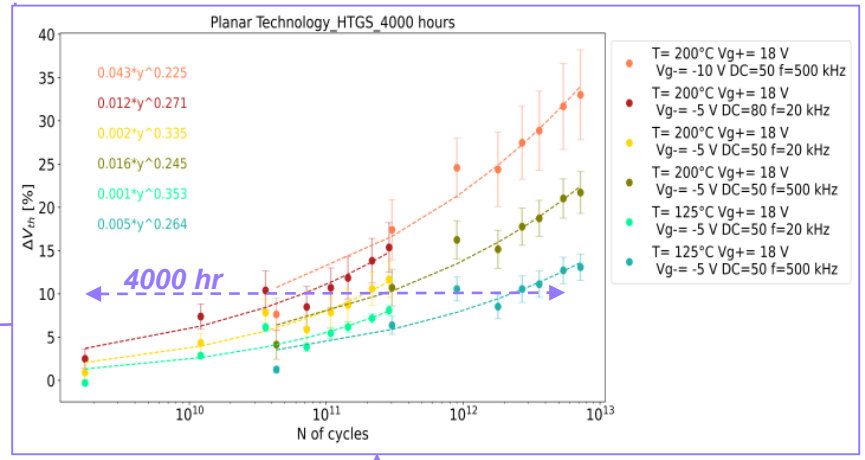
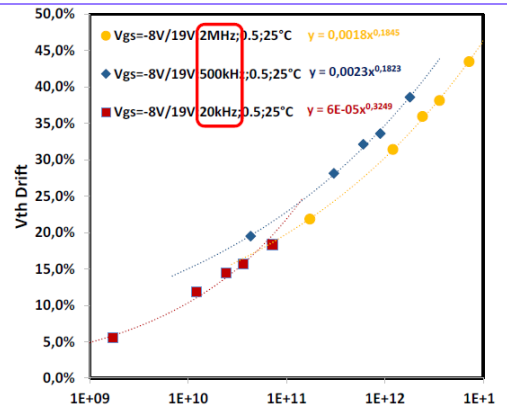


Figure 1 Ageing test and modeling process



Test Time 4000hr



No Frequency dependency (up to 2MHz)

NEW Model (Power-Law)

$$\Delta V_{th(GSS)} = A_0 \cdot \frac{1}{AF_T \cdot AF_{V+} \cdot AF_{V-}} \cdot N^{n_{stress} + \left[-\frac{\beta_T}{k_B}\frac{1}{T}\right] + exp(\beta_v V) - 1}$$

Power law as in Si, BUT differently from Si for SiC "n" is <u>not</u> constant AND depends form the "ageing" parameters (Vgs ,T) → Deep (in the oxide) traps are activated by higher Vgs stress.

β_T and β_v are new fitting parameters

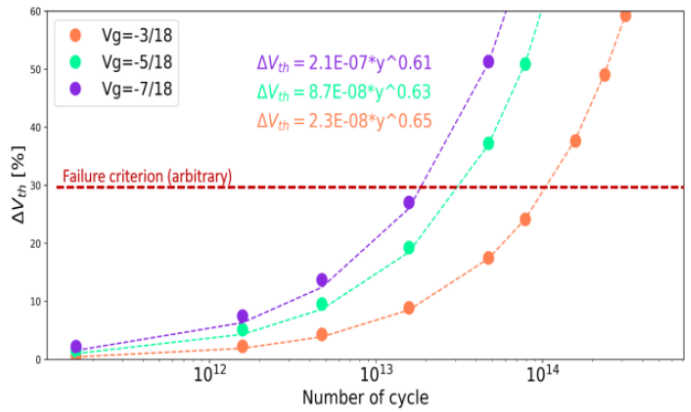


Figure 13 Vth drift estimation in function of number of cycle using the proposed model for inverter mission profile in automotive at 500 KHz and different *Vgs* for planar technology(Pl.1).

Table 3 Temperature profile for inverter (Automotive)

Tj [°C]	-25	0	25	50	75	100	125	150	175
op. hours [h]	263.8	103.1	594.6	1511.2	2239.1	1977.8	679.7	432.5	225.1

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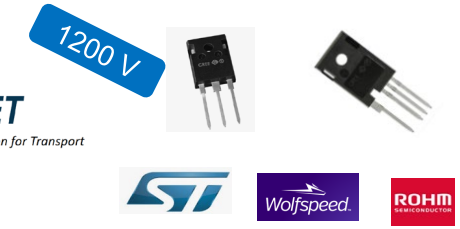
SICRET Program: From device to Module PoF

Structuring National and European SiC Industrial deployment (2019 – 2027)

Qualification Test plan Definition

User Guidelines definition (SOA, Design rules, …)

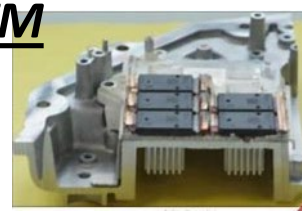
At discrete component level



At Power Module level including other studies/tests.

- Low pressure, humidity,
- Thermal management (power cycling, temperature cycling)
- EMC emission/immunity

Enhanced by the collaboration with STM (associate Partner of the project)



Source: ST Microelectronics

SiCRET +

Started on Nov 2023

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Lighthouse activities

Connecting with Specialized Networking

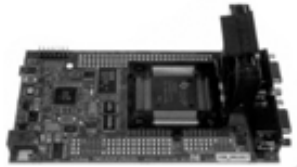
Thanks to the outcomes of the collaborative projects on reliability (SICRET/GANRET) high level scientific-technical initiatives have been engaged:

- Organization and active participation to WS on reliability of WBG devices (e.g. Expert Round tables, NRTW, ESREF…).
- Contribution to standard guidelines (e.g. AEQ324, JEDEC, AEC, …)
- Visibility at international level: European Center for Power Electronics (ECPE); Center for Power Electronic Systems (CPES) in USA

- Exchange and support international normalization bodies currently dealing with standardization of emerging WBG technologies, such as JEDEC, AEC, AFNOR, IEC…

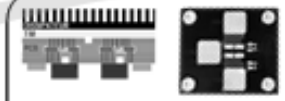
Technological & Methodological Levers

The big picture toward Electrification

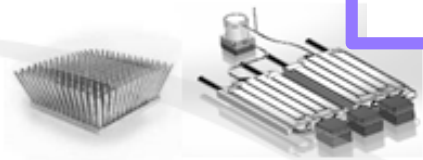


Optimized Control

WBG Power Module Integration



WBG PCB embedded



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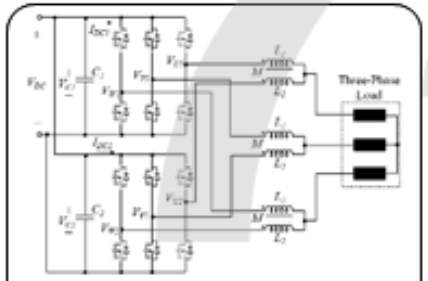

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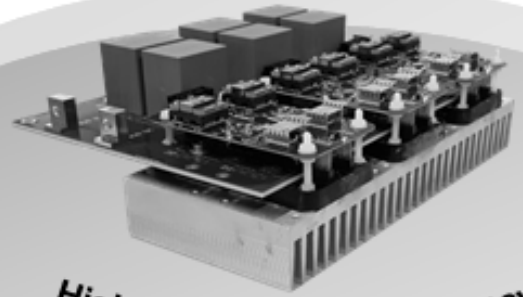
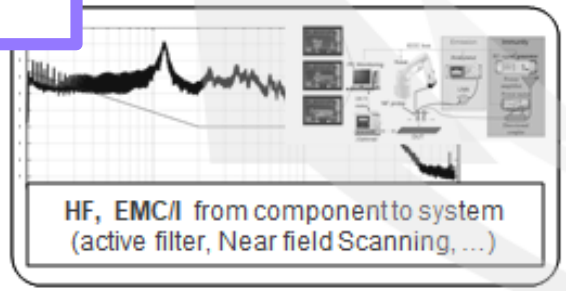


High Integration & Efficiency

High Dependability (harsh Envir / High constrain)

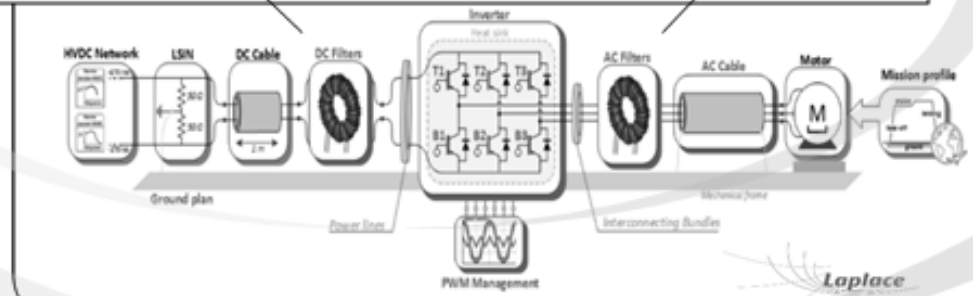
Failure Risk Assessment Methodology

RF Design and Modeling



HF, EMC/I from component to system
(active filter, Near field Scanning, ...)

Multidisciplinary Analysis / Optimization / Validation



In-System-Validation

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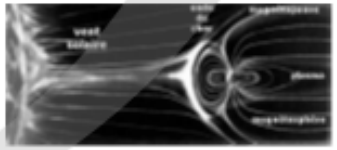
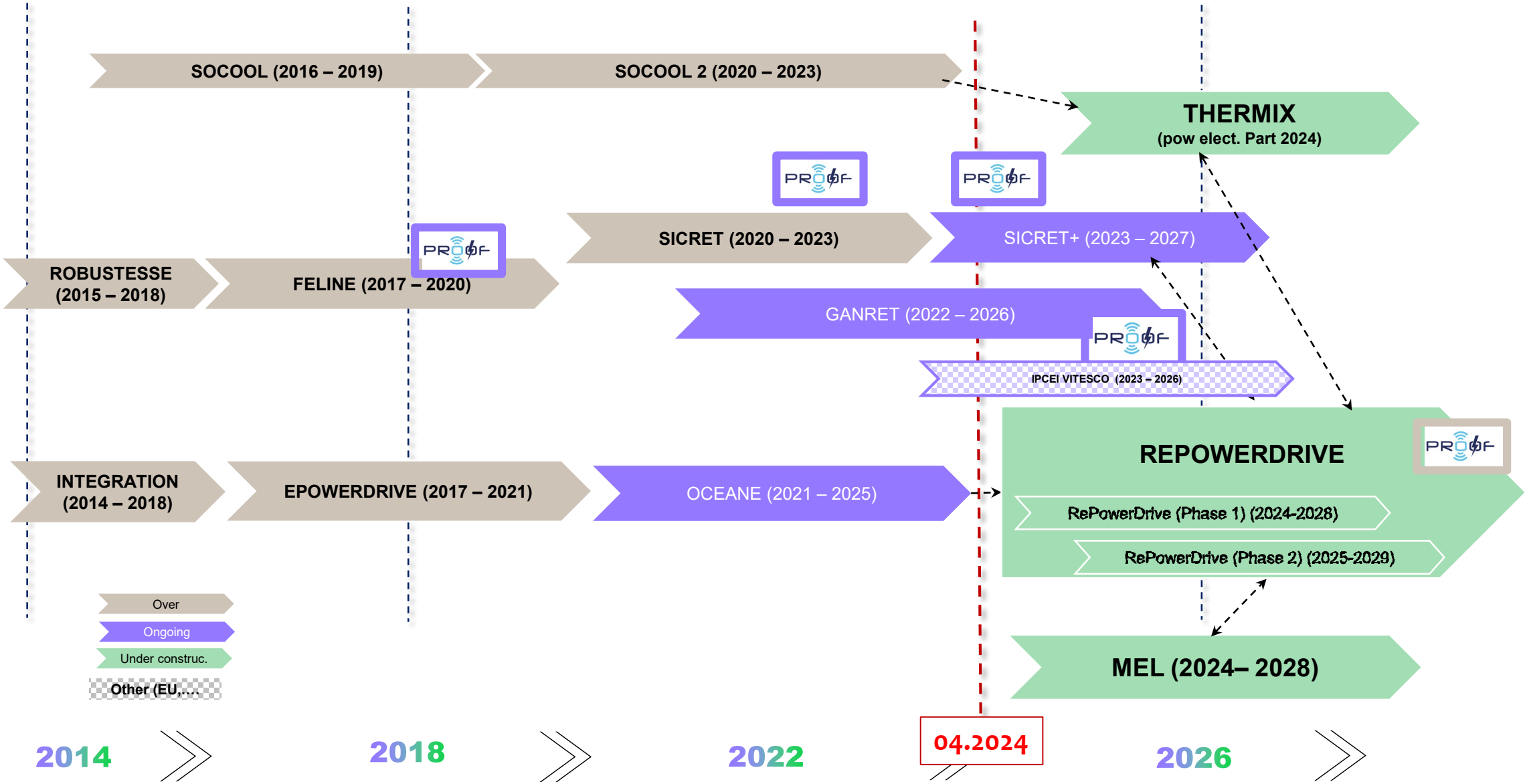


Cosmic radiation Immunity

HDRE Projects supporting roadmap (Status @ Q1-2024)

Comprehensive multi-sector and multidisciplinary program: focus on Power Electronics



Conclusions and Perspectives

- ✓ PROOF is an important part of the Regional / National R&D asset and roadmap (toward electrification)
- ✓ IRT-SE consider PROOF as an essential partner to reach critical mass in WBG reliability projects
- ✓ PROOF Scientific support (expertise and equipment) instrumental in running projects (e.g. SICRET, GANRET, …)

- ➢ Much more is ongoing and has to come yet:
  - Aging degradation physics modeling of WBG (beyond SiC and GaN)
  - Close the gap between power electronics and HF electronics (NFS, S-Param, …

Merci !

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