Original Design Procedure For Self-Reconfigurable Low Noise Figure and High RF Input Power Overdrive LNAs: Application To X-Band GaN MMICs

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***Abstract*—This article proposes an original method for designing Low Noise Amplifiers on wide-bandgap RF technologies. These LNAs are able to withstand high electromagnetic signals, like those used in electronic warfare, while providing high detectivity. The study presents the original design procedure of a single-stage LNA and a two-stage LNA based on the same strategy. These self-reconfigurable LNAs make it possible to switch from a high detectivity mode (low NF) to a high linearity mode (high input compression mode IP_{1dB}). This design strategy is compared to a robust LNA design, which uses a larger transistor size for improved linearity at the cost of a slight NF degradation. RF step-stress results has been performed up to 30 dBm at the input of the amplifier without any destruction, and providing stable S-parameters and noise figure.**

Keywords—GaN, MMIC LNA, robust receiver, self-reconfigurable LNA, highly linear, low NF, RF step stress.

I. Introduction

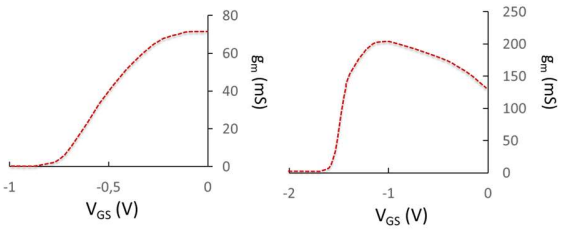
While LNAs based on CMOS technology suffer from a reduction of the supply voltage as a consequence of the reduction of the channel length (scaling of the CMOS voltage, i.e. [1]), and therefore a reduction of the maximum RF overdrive in linear mode or before destruction, wide bandgap technologies, such as Nitride technologies, open the way to the design of new amplifier architectures, mainly for power amplification. In the case of Low Noise Amplifiers (LNA), GaN High Electron Mobility Transistor (HEMT) allows both good detectivity (low Noise Figure at 50 Ω input matching - NF_{50}) and improved robustness against electromagnetic (EM) waves for applications in harsh environment. In addition, these technologies can withstand high temperatures and can be placed at a very close distance from the antenna. With the increasing complexity related to the integration of multiple TxRx modules in Active Electronically Scanned Array systems, the separation of the protection device (radar burn-trough) and the LNA represents a limitation in the available space, while the necessary use of the limiter (protection system) degrades the overall detectivity by at least 1 dB at 10 GHz. The development of MMIC LNAs capable of handling high RF powers paves the way to a new generation of receivers, also taking into account the limitation of space once these RF frontends are packaged. While designers have started designing robust LNA circuits based on Nitride technologies over the past decade, few different strategies have been proposed in the literature [2][3]. In these articles, the maximum RF power that can be applied to the input of the LNA is taken into account at the end of the design cycle (conventional approach), or at the beginning of this procedure when choosing the transistor [4]: an interesting solution first proposed by M. Rudolph uses a larger size HEMT to achieve better linearity at the cost of a slightly degraded NF_{50} compared to the classical method. For radar or for satellite telecommunication systems, high-power microwave effect degrades the Bit Error Rate (BER) [5], and ultimately can also damage the receiver system.

In the second section, the proposed design procedure is summarized and compared to the conventional design methodology. The third section presents the measured performances of scattering parameters, NF_{50} and input power compression IP_{1dB} for the single-stage LNAs under study: our approach is compared to that developped in [4]. Then RF step-stress results are proposed for the single-stage LNAs, extended to a two-stage LNA using our design strategy. A conclusion summarizes this work, with a comparison with state-of-the-art LNAs considering NF_{50} versus IP_{1dB} for Nitride technologies.

II. Design Procedure for (self)reconfigurable LNA: Low NF_{50} and High IP_{1dB}

A. General considerations of narrow bandgap technologies versus wide bandgap technologies

For every RF circuit design, it all starts at the transistor level: the selection of the size and bias of the HEMT is crucial for the final performance of the circuit (and we should add also for the evaluation of its lifetime, when considering the stresses it is subjected to and other SOA rules!). In this article, only general considerations are given for the design of a GaN LNA. Of course, from a MMIC technology provider to another one, the recipee should be managed in a different way and this is why only the principal advices are given. First, as we deal with an amplifier function, the transconductance gain g_m is primordial. Moreover g_m also impacts detectivity (or whatever noise model is used, the four noise parameters!). Fig. 1 compares the static transfer characteristics with the transconductance gain of a narrow bandgap III-V technology (ED02AH) and of a widebandgap N-V technology (D01GH) from OMMIC. It is obvious that the maximum g_m peaks near the threshold voltage



a) b)

Fig. 1. Static simulation of the transconductance profile versus V_{GS} for a narrow bandgap technology -*a*, and for a wide bandgap technology -*b* (resp. OMMIC ED02AH and D01GH).

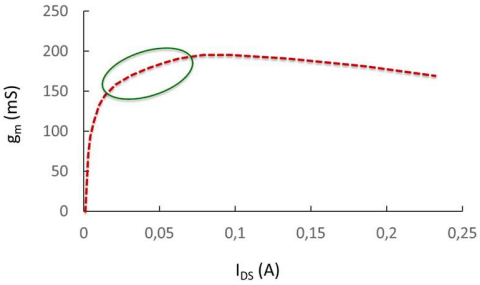


Fig. 2. Static simulation of the transconductance g_m versus I_{DS} for a 6x40 gate width HEMT biased at V_{DS}=5 V (OMMIC D01GH). In green circle is represented the optimum biasing zone for maximum gain and low noise.

for the GaN HEMT, while g_m decreases drastically for the III-V HEMT close to the pinchoff. Moreover, g_m is 10 times higher than for III-V HEMT at the optimum quiescent point for low noise applications (around $I_{DSS}/3$ for III-V, $I_{DSS}/5$ for N-V). Thus, the design of the two LNAs cannot be driven in the same way. Next, we consider the GaN technology. Whatever the transistor's noise model, the transconductance gain g_m, the resistance of the gate and of the source (R_S, R_G) or drain-source (R_{DS}) are the main parameters that play a role in the noise temperature or in the noise figure expression. Popiezalski's empirical model for the minimum achievable noise temperature T_{min} [6] is calculated by highlighting g_m, and finally expressed according to (1), in an expression very close to those that can be found in other related models. Also (2) proposes the minimum noise factor F_{min} based on Fukui's model [7]. This model, although originally developed for MESFETs, is still relevant for HEMT devices providing higher g_m and a reduction of R_S and R_G resistances. K_f coefficient is related to the channel material and gate length. Whatever these models, g_m plays a role in the noise equations, as well as the resistances R_G and R_S and C_{GS} capacitor. This determines the transistor selection in relation with electrical parameters (DC plots and S-parameters).

$$T_{min} = \frac{4\pi C_{GS} f}{g_m}\sqrt{\frac{R_i T_g T_d}{R_{DS}} + \left(\frac{2\pi C_{GS} f}{g_m}\frac{R_i T_d}{R_{DS}}\right)^2} + \left(\frac{2\pi C_{GS} f}{g_m}\right)^2 \frac{2R_i T_d}{R_{DS}} \quad (1)$$

$$F_{min} = 1 + K_f 2\pi C_{GS} f \sqrt{\frac{(R_G + R_S)}{g_m}} \quad (2)$$

Not shown in the direct expression of (1) and (2), the drain current I_{DS} generates noise, as can be seen in [8] from Cappy, and rewritten in (3) as a function of g_m. I_{DS} has to be kept at a lower value, but still with elevated g_m. This is one of the great interest of GaN technologies regarding the $g_m(V_{GS})$ profile near the pinchoff zone where g_m is maximum. Fig. 2 plots g_m versus I_{DS}, and the inflexion zone where g_m decreases for the lower I_{DS} quiescent points represents the optimum biasing condition to use. The quick decreasing of g_m on the lower I_{DS} zone must be avoided for model dispersion (process variations from DOE), and reliability purposes (sensitivity to positive or negative bias temperature instabilities PBTI/NBTI).

$$F_{min} = 1 + 2\sqrt{\frac{V_i}{E_C L}}\frac{2\pi C_{GS} f}{\sqrt{g_m}}\sqrt{(R_G + R_S)} \quad (3)$$

Finally, for circuit designers, the four noise parameters to consider yield the noise factor F as formalized in (4):

$$F = F_{min} + \frac{R_n}{G_S}\left|Y_S - Y_{opt}\right|^2 \quad (4)$$

Where R_n is the equivalent noise resistance, Y_S=G_S+j.B_S the source admittance and Y_{opt} the optimum noise admittance. Next noise figures are used, expressed in decibel as NF_{min}=10.log(F_{min}).

B. Design fundamentals versus new design flow

Below we summarize the LNA design steps by the conventional strategy, and by the approach adopted in this work. The gate length for all designs is 100 nm. For the conventional design flow, the first parameters to consider concern the noise and small-signal characteristics. Linearity and other considerations are taken into account only at the end, and they are usually satisfied in a multi-stage topology. The proposed strategy also integrates linearity at the very beginning of the LNA design process.

Conventional design flow : best NF_{50}

■ *Transistor selection (size/bias):*

-Minimize the noise of the amplifier NF_{50} regarding the source impedance matching (admittance Y_S) to approach NF_{min}.

-According to the frequency band, the noise resistance should be carefully considered.

-Use inductive serial feedback to meet small-signal and noise matching at the input.

■ *Design fundamentals:*

-Design the lumped/real elements (design kit) matching network at the input (source) and output (load) of the LNA: evaluation of passives (inductor/capacitor quality factor, line losses). Also considering the DOE (technological dispersion).

-DC power management. P_{DC} is usually low for LNA (drain current reduction is mandatory, still keeping g_m high), and then appears the conflict between NF and IIP3.

-once the MMIC achieved, evaluate the maximum RF overdrive before destruction.

These fundamental rules can be used to design the rugged LNAs as in [4], but considering the IP_{1dB} at the earlier step, as for NF_{min}. Improving IP_{1dB} comes with the price of

compromising noise and linearity. Next, the design flow is completed with linearity considerations.

Complete design flow : best NF_{50} and high IP_{1dB}

■ *Transistor selection.*

-A mapping is realized on the sizing/biasing of the HEMTs at the center frequency of 10 GHz as proposed in Fig. 3, considering NF_{min} and IP_{1dB}. The objective is to find a device capable of being tuned from the best NF_{min} to the highest IP_{1dB} by changing the only tunable parameter of the MMIC process: the quiescent point. The g_m is also checked to be at the same value when changing the DC bias to keep the small signal gain S_{21} stable when switching from high detectivity mode to high linearity mode (and vice versa). For this study, a 6x40µm gate width transistor has been selected operating at (V_{DS}, I_{DS}) of (5V, 50 mA) in high detectivity mode (NF_{min}=0.44 dB, IP_{1dB}=8 dBm) and (V_{DS}, I_{DS}) of (10 V, 120 mA) in high linearity mode (NF_{min}=0.87 dB, IP_{1dB}=15 dBm). The optimization on IP_{1dB} is achieved by increasing P_{DC}=V_{DS}.I_{DS}; increasing V_{DS} and keeping I_{DS} low enough allows a degradation of NF_{min} by only 0.4 dB between the two modes (cf. Fig. 1 and equ. 3). This is relatively small considering the 1 dB degradation of NF_{50} associated to the presence of a limiter, in conventional receivers.

-Evaluate the trap effects (by model if available, or by considering lag metrics on output characteristics) according to the selection of DC-biasing paths in the output characteristics. All other consideration is following the conventional design flow.

■ *Design fundamentals:*

-The first steps are very close to the conventional flow, but the input/output reflexion coefficient should be constant to allow a good matching whatever the operating mode of the LNA. Moreover, the inconditionnal stability should be efficient when changing the DC bias between these operating modes (and also considering the critical DC-path between those quiescent points). Special care is given to the robustness of the MMIC stability when changing the DC bias. Iterations should be done between topology and device selection if stability cannot be satisfied within DC-paths. The two-stage design accounts for all the noise and linearity budget from the first stage, and the biasing is performed on each of the two stages for a maximum of dynamic in IP_{1dB}.

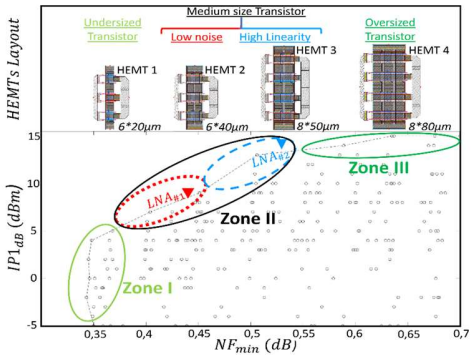


Fig. 3. Device biasing and sizing selection for Low Noise or high compression IP_{1dB} purposes (NFmin versus IP_{1dB} @10 GHz). Sizing is for number of gate fingers and gate individual width respectively ranging between [2;4;6;8] and [20 µm to 100 µm by step of 20 µm], while biasing on V_{GS} and V_{DS} respectively range between [-1,7 V to 0 V by step of 0.2 V] and [3 V;5 V;8 V;12 V;20 V]. The number of random sizing/DC biasing combinations is 1000.

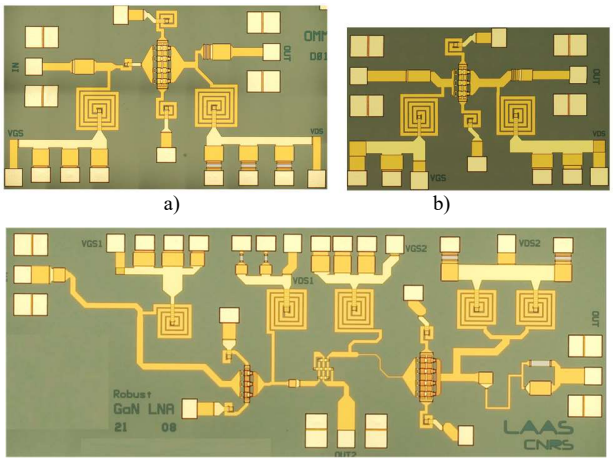
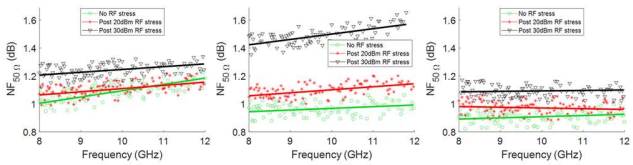


Fig. 4. Pictures of the a) single-stage rugged LNA (HEMT 8x50 µm biased at V_{DS}=12 V and I_{DS}=48 mA) and b) single-stage self-reconfigurable LNA (4x60µm biased at V_{DS}=5/10 V and I_{DS}=50/120 mA), and of the c) two-stage reconfigurable LNA. All LNAs operate in the 8 GHz - 12 GHz frequency band. Scales between circuits are respected.

-The maximum RF power rating is evaluated with the non-linear model and the SOA.

III. Measurement of the Self-Reconfigurable LNA and of the Rugged LNA

Two single-stage LNAs have been designed and measured; the rugged LNA featuring a large size HEMT (8x50 µm), and the self-reconfigurable LNA featuring a small size HEMT (6x40 µm) (resp. Fig. 3.a and Fig. 3.b). Special care has been given to the small-signal gain for self-reconfigurable LNAs, for which a constant gain is expected whatever the configuration. One two-stage LNA has been designed and measured [9], also self-reconfigurable but with a higher small-signal gain (>20 dB). All circuits are input/output matched with return loss lower than -10 dB over the 8 GHz - 12 GHz bandwidth. RF step-stresses have been performed up to 35 dBm at the input of the LNAs. No degradation on electrical and noise parameters occurs up to P_{in}=30 dBm [10]. Performances of 1-stage and 2-stage LNAs are summarized in Table I. Noise Figure measurements are performed with the PNA-X series 5244B from Keysight, option 029 (low noise measurement) for accurate measurement. Fig. 5 provides NF50 measurements over 8GHz-12GHz bandwidth for the LNAs under test.



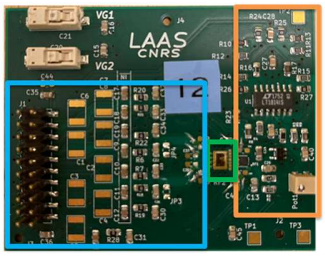
a) Rugged LNA & new strategy of LNA b) LN mode c) HL mode

Fig. 5. X-band noise figure measurements for the two 1-stage LNAs under test. a) NF50 for the rugged design. NF50 for the reconfigurable LNA under Low Noise operating mode b) and under High Linearity operating mode c). Measurements are performed at initial state t0 (green plots), and after different RF-step stresses: sequence #1 is after the P_{in}=20 dBm step stress (red plots) and sequence #2 is after the P_{in}=30 dBm step stress (black plots). Fatal failure occurs at P_{in}=35 dBm for all LNAs under test.

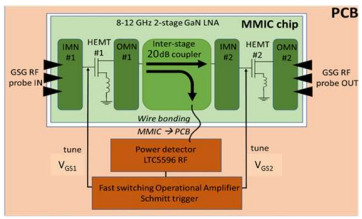
TABLE I. ELECTRICAL AND NOISE PERFORMANCE OF THE X-BAND MMIC LNAS

Type of LNA	Electrical and Noise performance between 8 GHz and 12 GHz				
	NF50 dB	***S_{21} dB***	***S_{11} / S_{22} dB***	***IP_{1dB} dBm no damage @ 10GHz***	***Max. RF input power dBm @ 10GHz***
1-stage rugged LNA	< 1.3	> 9	< -11 / < -14	+20	35
1-stage self-reconfigurable LNA (high detectivity / high linearity mode)	< 0.95 < 1.4	> 10 > 10	< -10 / < -11 < -10 / < -11	+4 +14	35 35
2-stage self-reconfigurable LNA (high detectivity / high linearity mode)	< 1.6 < 2.1	> 19 > 19	< -10 / < -11 < -10 / < -11	-5 +5	N.A

The LNA circuits support powers up to 20 dBm without degradation. A slight degradation occurs on NF50 for input power of 30 dBm (+0.5 dB and +0.2 dB / +0.1 dB respectively for 1-stage Rugged LNA and 1-stage reconfigurable LNA under Low Noise mode / High Linearity mode). The fatal failure appears at 35 dBm, concomitant with a rapid increase in the leakage current (all circuits show 10 mA gate leakage current at 30 dBm RF input power). Regardless of the design or bias strategy, the fatal failure appears to be related to the leakage current limitation of the Schottky gate, imposed by the technology-related operational safety zone, and device size or DC bias is not a first-order consideration. Fig. 6 depicts the PCB self-reconfigurating system with the power to DC converter and the MMIC chip (Fig. 6.a), as well as the synoptic of the whole system (Fig. 6.b). A full MMIC version has also been



a)



b)

Fig. 6. System with the MMIC chip reported on a PCB (a): picture of the MMIC chip in green rectangle, biasing circuit with power detector and Schmitt trigger in orange rectangle and medium to low frequency stability circuits in blue rectangle. The synoptic of the PCB and MMIC chipis given in (b) for the self-control of the biasing strategy between High-detectivity mode and High-linearity mode for the 2-stage LNA. The output pad of the single-stage LNAs or at the lange coupler situated between the two stages of the 2-stage LNA (MMIC) is connected to the RF to DC converter (power detector) by wire bonding. Then the DC signal is applied to a trigger of Schmitt. The hysteresis can be adjusted to select the two RF power thresholds (from high-detectivity mode to high-linearity protection mode, or from high-linearity to high-detectivity nominal mode).

successfully designed, with an integration as low as 2mm² chip. This fully integrated proof of concept should be of interest for robust self-reconfigurable receivers in AESA systems.

IV. CONCLUSIONS

This study compares different design versions of wide bandgap GaN MMIC LNAs operating in X-band. The conventional approach (high detectivity mode configuration) and the rugged design are compared to our self-reconfigurable design that offers flexibility between noise figure and input power at 1 dB compression. It is demonstrated that the receiver can adjust from a high detectivity mode to a protection mode by increasing IP_{1dB} by 10 dB (according to the detection of a critical EM signal level). One critical point during the design process of these GaN amplifiers concerns the unconditional stability to be achieved. We demonstrate that our self-reconfigurable LNA can operate safely on various DC quiescent points under CW RF signals. Also the pulsed biasing has been validated for all of the measured LNAs with rise and fall time of less than 30 µs. This makes the LNAs available for CW and for pulsed applications.

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